



# **Teseda V550™ DUT Card Design Guide**

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# 1 Overview

Prior to sending the request to the DUT card designer, the user must define how to fit the DUT requirements within the limitations of the Teseda V550 tester. The user should prepare the requirements for the following: pin voltage, output strobe time, and input clock timing. Additionally, the user should prepare the information for power supplies, high speed clocks and any on-board circuitry.

## 1.1 Pin voltage

The V550 has four major domains for pin voltage and timing. The domains are labeled A, B, C, and D and are physically connected to specific tester channels. As such, the user cannot assign a tester channel to a domain. For pin voltage, each of these domains is sub-divided into two sub-domains consisting of 64 tester channels. They are named A1, A2, B1, etc.

The user must sort all of the pins in their design by the pin voltage requirements, ensuring that the groups will fit in the 64bit sub-domains without overlapping. The V550 has four pin voltage families to choose from for LVCMOS 3.3V, LVCMOS 2.5V, LVCMOS 1.8V, and LVCMOS 1.5V IOs. Any other required voltages will require the use of level shifters on the DUT board.

## 1.2 Strobe timing

Next the user must sort the DUT pins by their timing requirements. The first timing requirement to consider is the strobe timing. Two strobe times can be defined for each major domain (A, B, C, and D). Each pin can select between these two strobe times for comparing the output value to the expected value in the test pattern. The pin list should now be sorted first by pin voltage and then by strobe time.

## 1.3 Clock timing

Clock timing is the next major consideration. For each domain, four clock pulses can be defined. These can be applied to any pin in that domain if it is selected as a clock. Waveforms can be defined that combine these pulses to produce multiple pulses within a single test cycle. For more information, see the “V550 Display Sample for Clocks” and “Simulating M Clocks using the V550 Tester” sections of the *Teseda OpenDFT WorkBench™ V500™ Series Hardware User’s Guide*.

## 1.4 Power Supplies

There are 8 DUT power supplies available on the V550. They are configured as defined in Table 1: DUT Power Supplies below:

**Table 1: DUT Power Supplies**

Supply Type	Voltage Range	Current Range	Qty.
High Current	600mV – 5. 0V	0A – 4A	4
Low Current	600mV – 5V	0A – 200mA	2
High Voltage	5V – 25V	0A – 30mA	1
Utility	5V		1

Additionally, the V550 can control external power supplies. Teseda recommends adding the ability to select an external power supply to replace an internal supply. In most cases, the connectors should be selected by the user and delivered to the DUT card designer. For four wire power supplies, a sense line is used to ensure accurate voltage delivery. This should be accounted for when the connector is chosen.

## 1.5 Other Circuitry

Finally, the high speed clocks and on-board circuitry need to be planned. There are four high-speed, free-running clocks available for operating PLLs and other such circuits. The user should specify which DUT pins or on-board circuits these need to be connected to.

## 2 Design

At this point, the user should have provided the DUT card designer with a list or table of pin groups determined by the criteria in section 1 along with the power supply information and additional circuitry. The DUT card designer must now finish the design. Although it is not strictly necessary, maintaining the DUT pin names in the DUT Card design will help to streamline the verification process.

### 2.1 Mechanical design

Figures 1 and 2 illustrate the mechanical design for the v550 DUT card. An AutoCad drawing file (DWG and DFX) is included in this v550 DUT Card Design kit. In addition to the AutoCad drawings, Gerber files for the top, and bottom layers and the drill layer for the through-hole connectors are included in the kit. These files are:

- Top Layer: EtchLayer1Top.gdo
- Bottom Layer: EtchLayer14Bottom.gdo
- Drill Drawing: DrillDrawingThrough.gdo

Figure 1: Tester-side Mechanical Drawing

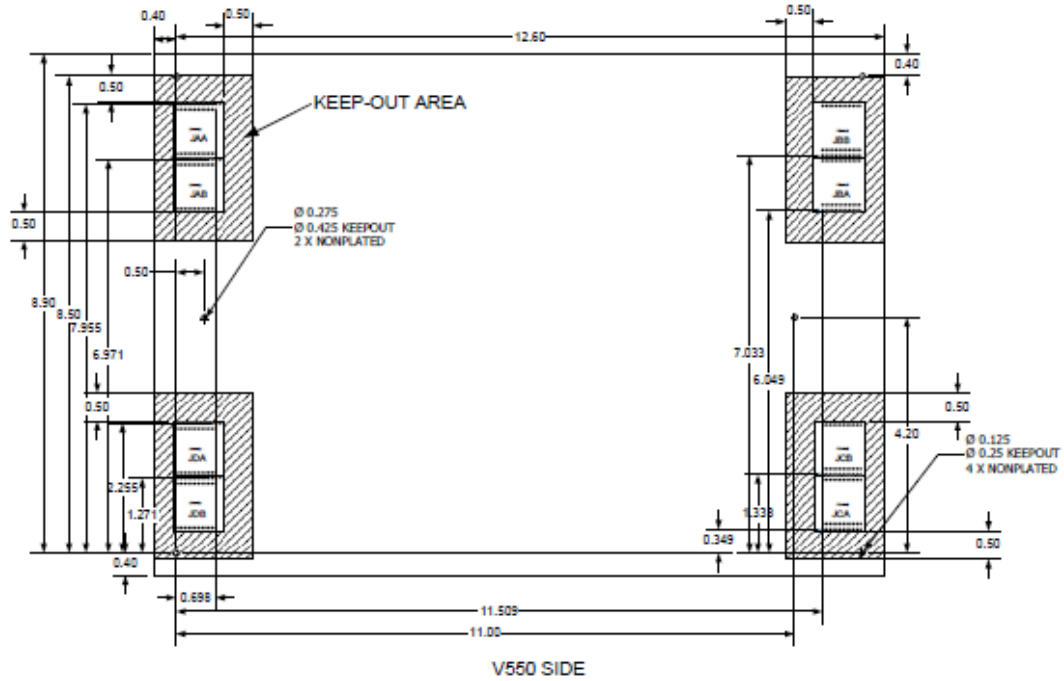
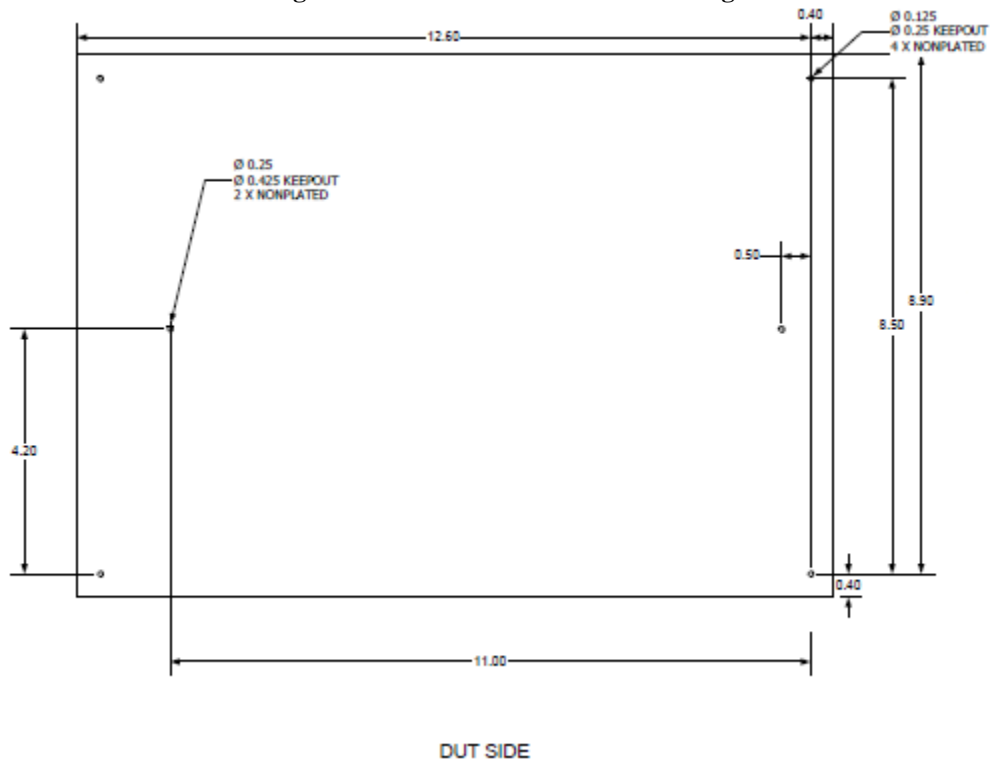


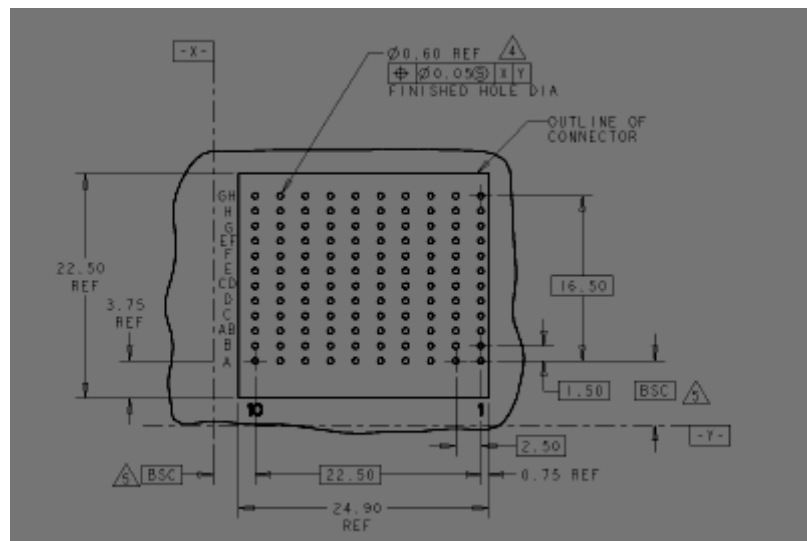
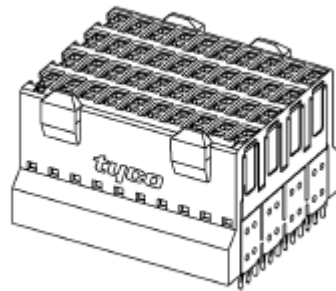
Figure 2: DUT-side Mechanical Drawing



## 2.1.1 Connectors for V550

The V550 uses eight Tyco HMZD connectors. These are configured in four banks with two connectors in each bank as illustrated in the previous section. Each connector bank provides the signals for one tester domain. The part number for the female connectors that are required on the DUT card is: 1469362-1. The figures below illustrate the connector and the board design to accommodate this connector. Mechanical drawings for this connector are included in this package in the file: female\_vertical\_HMZD\_C\_1469362\_O.pdf

Figure 3: V550 Connectors



## 2.1.2 Mechanical design rules

The following rules should be applied to all v550 DUT Cards:

The Maximum component height on the Tester side of the board is 0.2 inches.

Ensure that no components are within 1/2 inch of tester connectors on the bottom side of the board.

## 2.2 Electrical Design

The following electrical design rules and recommendations should be used for the V550.

### 2.2.1 Electrical Design Rules

The following guidelines should be applied to all DUT cards for the v550:

Use power planes and ground planes.

Allow no more than two signal layers to be stacked and only if routed orthogonally.

Maintain 50 Ohm transmission lines.

Maintain trace length matching within +/- 50 mil.

Add calibration test points close to the DUT with a trace length equivalent to signals. The calibration signals are defined in the signal descriptions in Section 2.3 of this document.

Add bulk capacitors at power supply connection (recommend 47uF Tantalum).

Add Decoupling capacitors as close to DUT power pin as possible (recommend a 0.1uF per power supply pin).

Add a frame ground to the board.

### 2.2.2 Electrical Design Recommendations

In addition to the stated design rules, we recommend the following:

Add cuttable traces to signals for addition of series termination resistors.

Add power connectors for external power supplies. Add a jumper circuit to select between the internal and external power supplies.

Add SMA connectors for triggers and fail signals.

## 2.3 V550 Signal Definitions

Table 2 below describes the signals of the V550 system:

**Table 2: V550 Signal Definitions**

Signal	Description
SCAN_IO [0:511]	Scan_IO[0:511] are IO channels to the DUT. These signals can be configured as a data IO or as a scan clock. The PMSU option allows PMU readings of all these signals.
DUT_CTRL [0:31]	Additional output signals that can be used to configure or place the DUT in a specific mode of operation. The value of these outputs doesn't change during the scan test. These signals are not accessed by the PMUs on the PMSU.
STRB_x_CAL_CMP	This signal is provided for calibrating the capture strobes for each domain. It reflects the captured signal back to the connectors for monitoring with an oscilloscope. This signal should be terminated with a testpoint.

Signal	Description
REF_x_CAL_OUT	This is a calibration signal that can be compared with the MASTER_CAL_REF by means of an oscilloscope to determine domain level phase shifting requirements.
SCOPE_x_TRIGGER	This signal provides a trigger for external test equipment. It will pulse on a user pre-defined scan cycle.
SCOPE_x_VECTOR_FAIL_PULSE	This signal will pulse when a failed vector is detected in its corresponding domain. It will pulse for one scan clock cycle.
SCOPE_x_VECTOR_FAIL_LATCH	This signal will pulse when a failed vector is detected in its corresponding domain. It will rise on a pre-determined failed vector number and remain high for the remainder of the scan test.
STRB_x_CAL_LPBK	See STRB_x_CAL_OUT
STRB_x_CAL_OUT	This signal is used for the calibration of the capture strobe of each domain. On the DUT card, this signal should have twice the length as the SCAN_IO signals and it should be routed back to the STRB_x_CAL_LPBK pin. A testpoint should be placed at mid-length of this trace for calibration purposes.
IDDQ_VOUT[x]	Part of QSTAR's IDDQ module interface. Should be connected to the VOUT pin of the QD1011 module.
IDDQ_CLK[x]	Part of QSTAR's IDDQ module interface. Should be connected to the CLK pin of the QD1011 module.
IDDQ_MD[x]	Part of QSTAR's IDDQ module interface. Should be connected to the MD pin of the QD1011 module.
IDDQ_RST	Part of QSTAR's IDDQ module interface. Should be connected to the RESET pin of the QD1011 module.
DUT_VER[0:2]	DUT card version pins for identification of a DUT card. These signals have internal Pull-ups and should be grounded to indicate a '0'.
DUTCARD_PRSENT#	This signal communicates to the V550 that the DUT card is plugged in. On the DUT card this signal should be grounded.
CLKGEN_OE[n]	OUTPUT ENABLE signal to a pair of the 4 possible high speed clock circuits.
CLKGEN_SLOAD[n]	LOAD signal to one of the 4 possible high speed clock circuits.
CLKGEN_SDATA	Shared SERIAL DATA signal to all 4 possible high speed clock circuits.
CLKGEN_SCLK	Shared SERIAL CLOCK signal to all 4 possible high speed clock circuits.
GLB_TRIGGER	This signal provides a trigger for external test equipment. It will pulse on a user pre-defined scan cycle. The trace should be terminated with a connector interface to the external equipment.
GLB_SCOPE_VCTR_FAIL	This signal will pulse when a failed vector is detected in any of the 4 domains. It will pulse for one scan clock cycle. The trace should be terminated with a connector interface to the external equipment.

Signal	Description
GLB_SCOPE_FAIL_LATCH	This signal will pulse when a failed vector is detected in any of the 4 domains. It will rise on a pre-determined failed vector number and remain high for the remainder of the scan test. The trace should be terminated with a connector interface to the external equipment.
MASTER_CAL_REF	This is master calibration reference signal. Any signal that needs calibration should use this signal as the reference. MASTER_CAL_REF should have the same length as the signal that needs to be calibrated. It should be terminated with a test point.
LO_CURR[x]_SENSEP	Sense line for the low current DUT power supply. Should be connected the LOW_CURR[x] at the load.
LO_CURR[x]	Low current DUT supply.
GATE_5V	Gated Utility 5V supply to power peripheral circuitry.
HI_CURR[x]	High current DUT supply.
HI_CURR[x]_SENSEN	Negative sense line for the low current DUT power supply. Should be connected to GND at the load.
HI_CURR[x]_SENSEP	Positive sense line for the low current DUT power supply. Should be connected to HI_CURR[x] at the load.
H_VOLTG_P	Positive High Voltage DUT Supply
FRAME GND	Frame Ground
RESERVED	These signals are reserved and should be left unconnected.

Table 3 describes the signal locations on the V550 connectors. This information is also available in the Excel spreadsheet included in this package.

**Table 3: v550 Pinout Table**

JA1	GH	H	G	EF	F	E
1	GND	Scan IO [7]	Scan IO [6]	GND	Scan IO [5]	Scan IO [4]
2	GND	Scan IO [15]	Scan IO [14]	GND	Scan IO [13]	Scan IO [12]
3	GND	Scan IO [23]	Scan IO [22]	GND	Scan IO [21]	Scan IO [20]
4	GND	Scan IO [31]	Scan IO [30]	GND	Scan IO [29]	Scan IO [28]
5	GND	Scan IO [39]	Scan IO [38]	GND	Scan IO [37]	Scan IO [36]
6	GND	Scan IO [47]	Scan IO [46]	GND	Scan IO [45]	Scan IO [44]
7	GND	Scan IO [55]	Scan IO [54]	GND	Scan IO [53]	Scan IO [52]
8	GND	Scan IO [63]	Scan IO [62]	GND	Scan IO [61]	Scan IO [60]
9	GND	Scan IO [71]	Scan IO [70]	GND	Scan IO [69]	Scan IO [68]
10	GND	Scan IO [79]	Scan IO [78]	GND	Scan IO [77]	Scan IO [76]

JA1	CD	D	C	AB	B	A
1	GND	Scan IO [3]	Scan IO [2]	GND	Scan IO [1]	Scan IO [0]
2	GND	Scan IO [11]	Scan IO [10]	GND	Scan IO [9]	Scan IO [8]

3	GND	Scan IO [19]	Scan IO [18]	GND	Scan IO [17]	Scan IO [16]
4	GND	Scan IO [27]	Scan IO [26]	GND	Scan IO [25]	Scan IO [24]
5	GND	Scan IO [35]	Scan IO [34]	GND	Scan IO [33]	Scan IO [32]
6	GND	Scan IO [43]	Scan IO [42]	GND	Scan IO [41]	Scan IO [40]
7	GND	Scan IO [51]	Scan IO [50]	GND	Scan IO [49]	Scan IO [48]
8	GND	Scan IO [59]	Scan IO [58]	GND	Scan IO [57]	Scan IO [56]
9	GND	Scan IO [67]	Scan IO [66]	GND	Scan IO [65]	Scan IO [64]
10	GND	Scan IO [75]	Scan IO [74]	GND	Scan IO [73]	Scan IO [72]

**JA2**

	GH	H	G	EF	F	E
1	GND	Scan IO [87]	Scan IO [86]	GND	Scan IO [85]	Scan IO [84]
2	GND	Scan IO [95]	Scan IO [94]	GND	Scan IO [93]	Scan IO [92]
3	GND	Scan IO [103]	Scan IO [102]	GND	Scan IO [101]	Scan IO [100]
4	GND	Scan IO [111]	Scan IO [110]	GND	Scan IO [109]	Scan IO [108]
5	GND	Scan IO [119]	Scan IO [118]	GND	Scan IO [117]	Scan IO [116]
6	GND	Scan IO [127]	Scan IO [126]	GND	Scan IO [125]	Scan IO [124]
7	GATE_5V	DUT_CTRL[24]	DUT_CTRL[25]	GATE_5V	DUT_CTRL[26]	DUT_CTRL[27]
8	GND	RESERVED	RESERVED	GND	RESERVED	RESERVED
9	HI_CURR[1]	RESERVED	RESERVED	HI_CURR[1]	RESERVED	RESERVED
10	GND	STRB_A_CAL_OUT	STRB_A_CAL_LP BK	GND	SCOPE_A_VECTOR_FAIL_LATCH	DDM_PRSNT#

**JA2**

	CD	D	C	AB	B	A
1	GND	Scan IO [83]	Scan IO [82]	GND	Scan IO [81]	Scan IO [80]
2	GND	Scan IO [91]	Scan IO [90]	GND	Scan IO [89]	Scan IO [88]
3	GND	Scan IO [99]	Scan IO [98]	GND	Scan IO [97]	Scan IO [96]
4	GND	Scan IO [107]	Scan IO [106]	GND	Scan IO [105]	Scan IO [104]
5	GND	Scan IO [115]	Scan IO [114]	GND	Scan IO [113]	Scan IO [112]
6	GND	Scan IO [123]	Scan IO [122]	GND	Scan IO [121]	Scan IO [120]
7	GATE_5V	DUT_CTRL[28]	DUT_CTRL[29]	GATE_5V	DUT_CTRL[30]	DUT_CTRL[31]
8	GND	RESERVED	RESERVED	GND	RESERVED	RESERVED
9	HI_CURR[1]	RESERVED	RESERVED	HI_CURR[1]	RESERVED	RESERVED
10	GND	SCOPE_A_VECTOR_FAIL_PULSE	SCOPE_A_TRIGGER	GND	REF_A_CAL_OUT	STRB_A_CAL_CMP

**JB1**

	A	B	AB	C	D	CD
10	Scan IO [200]	Scan IO [201]	GND	Scan IO [202]	Scan IO [203]	GND
9	Scan IO [192]	Scan IO [193]	GND	Scan IO [194]	Scan IO [195]	GND
8	Scan IO [184]	Scan IO [185]	GND	Scan IO [186]	Scan IO [187]	GND
7	Scan IO [176]	Scan IO [177]	GND	Scan IO [178]	Scan IO [179]	GND
6	Scan IO [168]	Scan IO [169]	GND	Scan IO [170]	Scan IO [171]	GND

5	Scan IO [160]	Scan IO [161]	GND	Scan IO [162]	Scan IO [163]	GND
4	Scan IO [152]	Scan IO [153]	GND	Scan IO [154]	Scan IO [155]	GND
3	Scan IO [144]	Scan IO [145]	GND	Scan IO [146]	Scan IO [147]	GND
2	Scan IO [136]	Scan IO [137]	GND	Scan IO [138]	Scan IO [139]	GND
1	Scan IO [128]	Scan IO [129]	GND	Scan IO [130]	Scan IO [131]	GND

JB1	E	F	EF	G	H	GH
10	Scan IO [204]	Scan IO [205]	GND	Scan IO [206]	Scan IO [207]	GND
9	Scan IO [196]	Scan IO [197]	GND	Scan IO [198]	Scan IO [199]	GND
8	Scan IO [188]	Scan IO [189]	GND	Scan IO [190]	Scan IO [191]	GND
7	Scan IO [180]	Scan IO [181]	GND	Scan IO [182]	Scan IO [183]	GND
6	Scan IO [172]	Scan IO [173]	GND	Scan IO [174]	Scan IO [175]	GND
5	Scan IO [164]	Scan IO [165]	GND	Scan IO [166]	Scan IO [167]	GND
4	Scan IO [156]	Scan IO [157]	GND	Scan IO [158]	Scan IO [159]	GND
3	Scan IO [148]	Scan IO [149]	GND	Scan IO [150]	Scan IO [151]	GND
2	Scan IO [140]	Scan IO [141]	GND	Scan IO [142]	Scan IO [143]	GND
1	Scan IO [132]	Scan IO [133]	GND	Scan IO [134]	Scan IO [135]	GND

JB2	A	B	AB	C	D	CD
10	STRB_B_CAL_CMP	REF_B_CAL_OUT	GND	SCOPE_B_TRIGGER	SCOPE_B_VECTOR_FAIL_PULSE	GND
9	RESERVED	RESERVED	HI_CURR[2]	RESERVED	RESERVED	HI_CURR[2]
8	IDDQ_VOUT[1]	IDDQ_VOUT[2]	LO_CURR[1]	IDDQ_CLK[1]	IDDQ_CLK[2]	LO_CURR[1]
7	DUT_CTRL[23]	DUT_CTRL[22]	LO_CURR[2]	DUT_CTRL[21]	DUT_CTRL[20]	LO_CURR[2]
6	Scan IO [248]	Scan IO [249]	GND	Scan IO [250]	Scan IO [251]	GND
5	Scan IO [240]	Scan IO [241]	GND	Scan IO [242]	Scan IO [243]	GND
4	Scan IO [232]	Scan IO [233]	GND	Scan IO [234]	Scan IO [235]	GND
3	Scan IO [224]	Scan IO [225]	GND	Scan IO [226]	Scan IO [227]	GND
2	Scan IO [216]	Scan IO [217]	GND	Scan IO [218]	Scan IO [219]	GND
1	Scan IO [208]	Scan IO [209]	GND	Scan IO [210]	Scan IO [211]	GND

JB2	E	F	EF	G	H	GH
10	DUTCARD_PRSNT#	SCOPE_B_VECTOR_FAIL_LATCH	GND	STRB_B_CAL_LPBK	STRB_B_CAL_OUT	GND
9	RESERVED	DUT_VER[2]	HI_CURR[2]	DUT_VER[1]	DUT_VER[0]	HI_CURR[2]
8	IDDQ_MD[1]	IDDQ_MD[2]	LO_CURR[1]	IDDQ_RST		LO_CURR[1]
7	DUT_CTRL[19]	DUT_CTRL[18]	LO_CURR[2]	DUT_CTRL[17]	DUT_CTRL[16]	LO_CURR[2]
6	Scan IO [252]	Scan IO [253]	GND	Scan IO [254]	Scan IO [255]	GND
5	Scan IO [244]	Scan IO [245]	GND	Scan IO [246]	Scan IO [247]	GND

4	Scan IO [236]	Scan IO [237]	GND	Scan IO [238]	Scan IO [239]	GND
3	Scan IO [228]	Scan IO [229]	GND	Scan IO [230]	Scan IO [231]	GND
2	Scan IO [220]	Scan IO [221]	GND	Scan IO [222]	Scan IO [223]	GND
1	Scan IO [212]	Scan IO [213]	GND	Scan IO [214]	Scan IO [215]	GND

**JC1**

	A	B	AB	C	D	CD
10	Scan IO [328]	Scan IO [329]	GND	Scan IO [330]	Scan IO [331]	GND
9	Scan IO [320]	Scan IO [321]	GND	Scan IO [322]	Scan IO [323]	GND
8	Scan IO [312]	Scan IO [313]	GND	Scan IO [314]	Scan IO [315]	GND
7	Scan IO [304]	Scan IO [305]	GND	Scan IO [306]	Scan IO [307]	GND
6	Scan IO [296]	Scan IO [297]	GND	Scan IO [298]	Scan IO [299]	GND
5	Scan IO [288]	Scan IO [289]	GND	Scan IO [290]	Scan IO [291]	GND
4	Scan IO [280]	Scan IO [281]	GND	Scan IO [282]	Scan IO [283]	GND
3	Scan IO [272]	Scan IO [273]	GND	Scan IO [274]	Scan IO [275]	GND
2	Scan IO [264]	Scan IO [265]	GND	Scan IO [266]	Scan IO [267]	GND
1	Scan IO [256]	Scan IO [257]	GND	Scan IO [258]	Scan IO [259]	GND

**JC1**

	E	F	EF	G	H	GH
10	Scan IO [332]	Scan IO [333]	GND	Scan IO [334]	Scan IO [335]	GND
9	Scan IO [324]	Scan IO [325]	GND	Scan IO [326]	Scan IO [327]	GND
8	Scan IO [316]	Scan IO [317]	GND	Scan IO [318]	Scan IO [319]	GND
7	Scan IO [308]	Scan IO [309]	GND	Scan IO [310]	Scan IO [311]	GND
6	Scan IO [300]	Scan IO [301]	GND	Scan IO [302]	Scan IO [303]	GND
5	Scan IO [292]	Scan IO [293]	GND	Scan IO [294]	Scan IO [295]	GND
4	Scan IO [284]	Scan IO [285]	GND	Scan IO [286]	Scan IO [287]	GND
3	Scan IO [276]	Scan IO [277]	GND	Scan IO [278]	Scan IO [279]	GND
2	Scan IO [268]	Scan IO [269]	GND	Scan IO [270]	Scan IO [271]	GND
1	Scan IO [260]	Scan IO [261]	GND	Scan IO [262]	Scan IO [263]	GND

**JC2**

	A	B	AB	C	D	CD
10	STRB_C_CAL_CMP	REF_C_CAL_OUT	GND	SCOPE_C_TRIGGE R	SCOPE_C_VECTOR_FAIL_PULSE	GND
9	CLKGEN_SD ATA	CLKGEN_SCLK	HI_CURR[3]	CLKGEN_CLK25P	CLKGEN_CLK25N	HI_CURR[3]
8			Reserved	CLKGEN_OE[3_4]	CLKGEN_OE[1_2]	Reserved
7	DUT_CTRL[1 5]	DUT_CTRL[14]	H_VLTG_P	DUT_CTRL[13]	DUT_CTRL[12]	H_VLTG_P
6	Scan IO [376]	Scan IO [377]	GND	Scan IO [378]	Scan IO [379]	GND
5	Scan IO [368]	Scan IO [369]	GND	Scan IO [370]	Scan IO [371]	GND
4	Scan IO [360]	Scan IO [361]	GND	Scan IO [362]	Scan IO [363]	GND
3	Scan IO [352]	Scan IO [353]	GND	Scan IO [354]	Scan IO [355]	GND

2	Scan IO [344]	Scan IO [345]	GND	Scan IO [346]	Scan IO [347]	GND
1	Scan IO [336]	Scan IO [337]	GND	Scan IO [338]	Scan IO [339]	GND

**JC2**

	E	F	EF	G	H	GH
10	RESERVED	SCOPE_C_VECTOR_FAIL_LATCH	GND	STRB_C_CAL_LPB K	STRB_C_CAL_OUT	GND
9	RESERVED	RESERVED	HI_CURR[3]	RESERVED	RESERVED	HI_CURR[3]
8	CLKGEN_SLOAD[4]	CLKGEN_SLOAD[3]	Reserved	CLKGEN_SLOAD[2]	CLKGEN_SLOAD[1]	Reserved
7	DUT_CTRL[11]	DUT_CTRL[10]	H_VLTG_P	DUT_CTRL[9]	DUT_CTRL[8]	H_VLTG_P
6	Scan IO [380]	Scan IO [381]	GND	Scan IO [382]	Scan IO [383]	GND
5	Scan IO [372]	Scan IO [373]	GND	Scan IO [374]	Scan IO [375]	GND
4	Scan IO [364]	Scan IO [365]	GND	Scan IO [366]	Scan IO [367]	GND
3	Scan IO [356]	Scan IO [357]	GND	Scan IO [358]	Scan IO [359]	GND
2	Scan IO [348]	Scan IO [349]	GND	Scan IO [350]	Scan IO [351]	GND
1	Scan IO [340]	Scan IO [341]	GND	Scan IO [342]	Scan IO [343]	GND

**JD1**

	GH	H	G	EF	F	E
1	GND	Scan IO [391]	Scan IO [390]	GND	Scan IO [389]	Scan IO [388]
2	GND	Scan IO [399]	Scan IO [398]	GND	Scan IO [397]	Scan IO [396]
3	GND	Scan IO [407]	Scan IO [406]	GND	Scan IO [405]	Scan IO [404]
4	GND	Scan IO [415]	Scan IO [414]	GND	Scan IO [413]	Scan IO [412]
5	GND	Scan IO [423]	Scan IO [422]	GND	Scan IO [421]	Scan IO [420]
6	GND	Scan IO [431]	Scan IO [430]	GND	Scan IO [429]	Scan IO [428]
7	GND	Scan IO [439]	Scan IO [438]	GND	Scan IO [437]	Scan IO [436]
8	GND	Scan IO [447]	Scan IO [446]	GND	Scan IO [445]	Scan IO [444]
9	GND	Scan IO [455]	Scan IO [454]	GND	Scan IO [453]	Scan IO [452]
10	GND	Scan IO [463]	Scan IO [462]	GND	Scan IO [461]	Scan IO [460]

**JD1**

	CD	D	C	AB	B	A
1	GND	Scan IO [387]	Scan IO [386]	GND	Scan IO [385]	Scan IO [384]
2	GND	Scan IO [395]	Scan IO [394]	GND	Scan IO [393]	Scan IO [392]
3	GND	Scan IO [403]	Scan IO [402]	GND	Scan IO [401]	Scan IO [400]
4	GND	Scan IO [411]	Scan IO [410]	GND	Scan IO [409]	Scan IO [408]
5	GND	Scan IO [419]	Scan IO [418]	GND	Scan IO [417]	Scan IO [416]
6	GND	Scan IO [427]	Scan IO [426]	GND	Scan IO [425]	Scan IO [424]
7	GND	Scan IO [435]	Scan IO [434]	GND	Scan IO [433]	Scan IO [432]
8	GND	Scan IO [443]	Scan IO [442]	GND	Scan IO [441]	Scan IO [440]
9	GND	Scan IO [451]	Scan IO [450]	GND	Scan IO [449]	Scan IO [448]
10	GND	Scan IO [459]	Scan IO [458]	GND	Scan IO [457]	Scan IO [456]

JD2	GH	H	G	EF	F	E
1	GND	Scan IO [471]	Scan IO [470]	GND	Scan IO [469]	Scan IO [468]
2	GND	Scan IO [479]	Scan IO [478]	GND	Scan IO [477]	Scan IO [476]
3	GND	Scan IO [487]	Scan IO [486]	GND	Scan IO [485]	Scan IO [484]
4	GND	Scan IO [495]	Scan IO [494]	GND	Scan IO [493]	Scan IO [492]
5	GND	Scan IO [503]	Scan IO [502]	GND	Scan IO [501]	Scan IO [500]
6	GND	Scan IO [511]	Scan IO [510]	GND	Scan IO [509]	Scan IO [508]
7	FRAME GND	DUT_CTRL[0]	DUT_CTRL[1]	FRAME GND	DUT_CTRL[2]	DUT_CTRL[3]
8	GND	RESERVED	RESERVED	GND	RESERVED	RESERVED
9	HI_CURR[4]	GLB_SCOPE_FAIL_LATCH	GLB_SCOPE_VCTR_FAIL	HI_CURR[4]	GLB_TRIGGER	
10	GND	STRB_D_CAL_OUT	STRB_D_CAL_LPBK	GND	SCOPE_D_VECTOR_FAIL_LATCH	MASTER_CAL_REF

JD2	CD	D	C	AB	B	A
1	GND	Scan IO [467]	Scan IO [466]	GND	Scan IO [465]	Scan IO [464]
2	GND	Scan IO [475]	Scan IO [474]	GND	Scan IO [473]	Scan IO [472]
3	GND	Scan IO [483]	Scan IO [482]	GND	Scan IO [481]	Scan IO [480]
4	GND	Scan IO [491]	Scan IO [490]	GND	Scan IO [490]	Scan IO [488]
5	GND	Scan IO [499]	Scan IO [498]	GND	Scan IO [497]	Scan IO [496]
6	GND	Scan IO [507]	Scan IO [506]	GND	Scan IO [505]	Scan IO [504]
7	FRAME GND	DUT_CTRL[4]	DUT_CTRL[5]	FRAME GND	DUT_CTRL[6]	DUT_CTRL[7]
8	GND	HI_CURR_SENSEN	HI_CURR_SENSEN	GND	HI_CURR[1]_SENSEP	HI_CURR[2]_SENSEP
9	HI_CURR[4]	LO_CURR[1]_SENSEP	LO_CURR[2]_SENSEP	HI_CURR[4]	HI_CURR[3]_SENSEP	HI_CURR[4]_SENSEP
10	GND	SCOPE_D_VECTOR_FAIL_PULSE	SCOPE_D_TRIGGER	GND	REF_D_CAL_OUT	STRB_D_CAL_CMP

### 3 Additional Items

This section includes additional items relating to how the V550 works in relation to IDDQ, self-test, and high speed clocks.

### **3.1 *IDDQ***

IDDQ is measured using QD-1011 IDDQ monitors from Q-Star. The V550 supports operating two of these monitors to facilitate testing quiescent current on two power supplies. The TWB software directly controls the monitor to apply the test and capture the results. There are dedicated signals that must be routed to the monitor and the power plane for the DUT must be separated from the tester power supply in order to facilitate the measurement. More information regarding this monitor can be obtained at [www.qstar.be](http://www.qstar.be). The following figures illustrate the connection requirements for the monitors:

Figure 4: QD-111 Application Diagram (Courtesy of Q-Star Belgium)

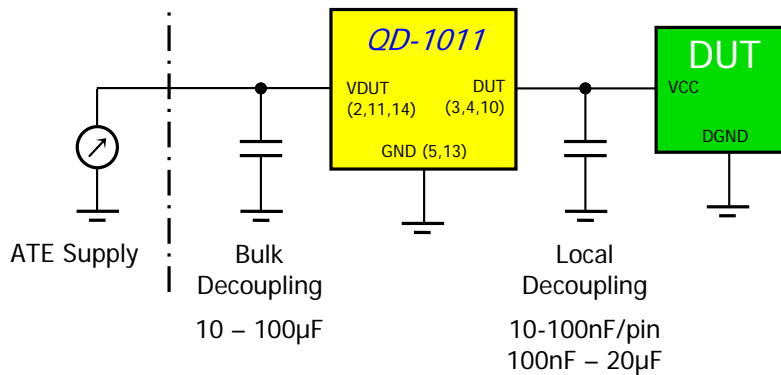
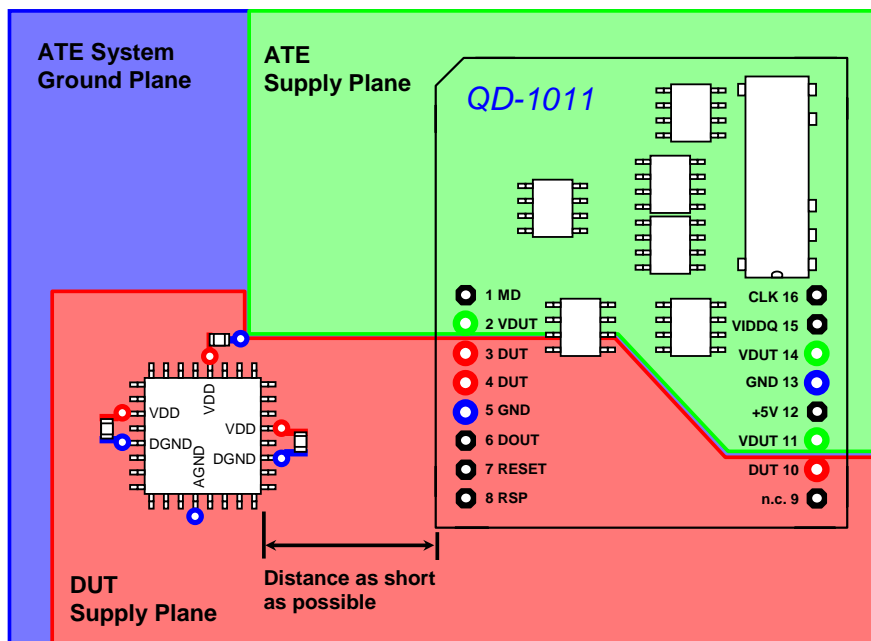


Figure 5: QD-1022 Power Plane Diagram (Courtesy of Q-Star Belgium)



The following table illustrates the connections for using the QD1011 IDDQ monitor on the V550.

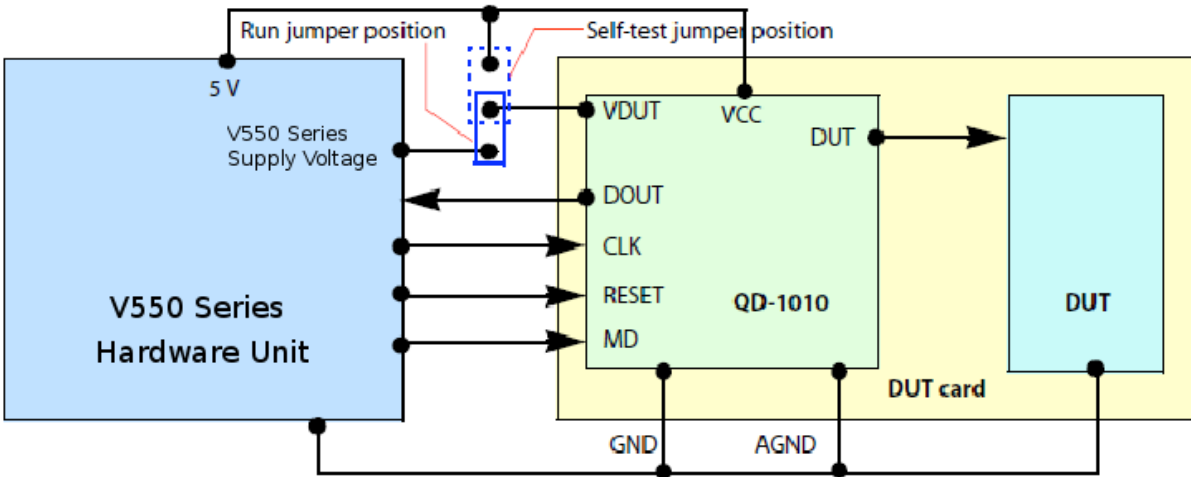
**Table 4: QD1011 IDDQ Monitor**

<b>QD-1011 pin name</b>	<b>QD-1011 pin number</b>	<b>V550 Signal</b>	<b>V550 Pin</b>	<b>DUT Card Connection</b>
MD	1	IDDQ_MD[1]	JB2-8E	
MD	1	IDDQ_MD[2]	JB2-8F	
VDUT	2	Power Supply n		Tester Supply plane
DUT	3	NC		DUT Supply Plane
DUT	4	NC		DUT Supply Plane
GND	5	Ground		Ground
DOUT	6	IDDQ_VOUT[1]	JB2-8A	
DOUT	6	IDDQ_VOUT[2]	JB2-8B	
RESET	7	IDDQ_RST	JB2-8G	
NC	8	NC		
NC	9	NC		
DUT	10	NC		DUT Supply Plane
VDUT	11	Power Supply n		Tester Supply plane
VCC	12	5V Power (Utility)	JA2-7GH	
GND	13	Ground		Ground
VDUT	14	Power Supply n		Tester Supply plane
VIDDQ	15	NC		
CLK	16	IDDQ_CLK[1]	JB2-8C	
CLK	16	IDDQ_CLK[2]	JB2-8D	

### 3.1.1 QD-1011 Self Test

The QD-1011 Monitors contain a self test feature that allows the user to verify that they are working properly before attempting to measure DUT currents. To facilitate this test, the board must have a jumper installed so the user can select either the DUT Power supply or the 5V Utility power supply as the source of the VDUT pin on the QD\_1011. This is illustrated in Figure 6: Self Test.

Figure 6: Self Test



### 3.2 High speed Clocks

The V550 can provide control to up to four ICS84330 frequency synthesizers to provide high speed clock signals of up to 700MHz to the DUT. These clocks are frequently used for BIST applications. The frequency synthesizers must be placed on the DUT card with the programming and control signals routed to the appropriate dedicated pins on the V550. A 16MHz crystal oscillator will be required to provide the reference frequency to the ICS84330. Please refer to the datasheet for the ICS84330, which is included in this package for more information. Since these devices produce a 3.3V LVPECL differential output signal, an additional buffer chip may be required to produce the single ended clock at the appropriate logic levels. The following table details the connections required for controlling the ICS84330 frequency synthesizers with the V550.

**Table 5: ICS84330 Frequency Synthesizer Connections**

V550 Pin Name	V550 Pin	Function	ICS84330 Pin Name
CLKGEN_SCLK	JC2-9B	Serial data clock	S_CLOCK **
CLKGEN_SDATA	JC2-9A	Serial data line	S_DATA **
CLKGEN_SLOAD[1]	JC2-8H	HS clock 1 program enable	S_LOAD
CLKGEN_OE[1]	JC2-8D	HS clock 1 output enable	OE
CLKGEN_SLOAD[2]	JC2-8G	HS clock 2 program enable	S_LOAD
CLKGEN_OE[2]	JC2-8D	HS clock 2 output enable	OE
CLKGEN_SLOAD[3]	JC2-8F	HS clock 3 program enable	S_LOAD
CLKGEN_OE[3]	JC2-8C	HS clock 3 output enable	OE
CLKGEN_SLOAD[4]	JC2-8E	HS clock 4 program enable	S_LOAD
CLKGEN_OE[4]	JC2-8C	HS clock 4 output enable	OE

\*\*Connect to all ICS84330 modules.

### 3.3 Timing Calibration

Each V550 is calibrated to ensure that the edge placements at the tester connector all occur within 1.5ns of each other. This factory calibration does not account for propagation delays that occur on the DUT card. To ensure the accuracy of the timing applied to the DUT two things must occur: the trace lengths of the signals must be matched as defined in section 2.2.1, and the propagation delay for the matched signals must be calibrated out of the test. In other words, the timing driven from the tester will be offset to account for the DUT card propagation delays.

To calibrate the DUT Card offset, dedicated loopback traces are placed on the DUT card that are twice the length of the SCAN\_IO signals. There is one pair of dedicated signals for each domain on the V550 as illustrated in the table below.

**Table 6: Calibration Signals**

V550 Signal	V550 Pin	Routing Guideline
STRB_A_CAL_OUT	JA2-10H	Connect to STRB_A_CAL_LPBK with trace that is twice the length of the SCAN_IO traces.
STRB_A_CAL_LPBK	JA2-10G	
STRB_B_CAL_OUT	JB2-10H	Connect to STRB_A_CAL_LPBK with trace that is twice the length of the SCAN_IO traces.
STRB_B_CAL_LPBK	JB2-10G	
STRB_C_CAL_OUT	JC2-10H	Connect to STRB_A_CAL_LPBK with trace that is twice the length of the SCAN_IO traces.
STRB_C_CAL_LPBK	JC2-10G	
STRB_D_CAL_OUT	JD2-10H	Connect to STRB_A_CAL_LPBK with trace that is twice the length of the SCAN_IO traces.
STRB_D_CAL_LPBK	JD2-10G	

### 3.4 Other Useful Signals

The following table shows other useful signals that may be displayed on the V550.

**Table 7: Other Useful Signals**

V550 Signal	V550 Pin	Req.	Description.
DUTCARD_PRSENT#	JB2-10E	Yes	Indicates that DUT card is present. Connect to ground.
DUT_VER[0]	JB2-9H	No	Signals designate the version of the DUT. These are pulled up on the tester and can be tied to ground to indicate a version number from 0 to 7.
DUT_VER[1]	JB2-9G	No	
DUT_VER[2]	JB2-9F	No	
GLB_SCOPE_VCTR_FAIL	JD2-9G	No	
GLB_SCOPE_FAIL_LATCH	JD2-9H	No	
SCOPE_A_TRIGGER	JA2-IOC	No	These signals are used to drive external equipment for Failure Analysis. They may be routed to the SMA connectors on the back of the tester or to SMA connectors on the DUT card.
SCOPE_B_TRIGGER	JB2-IOC	No	
SCOPE_C_TRIGGER	JC2-IOC	No	
SCOPE_D_TRIGGER	JD2-IOC	No	