



# Teseda V520™ DUT Card Design Guide

October, 2008



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# Designing a DUT Card for the V520

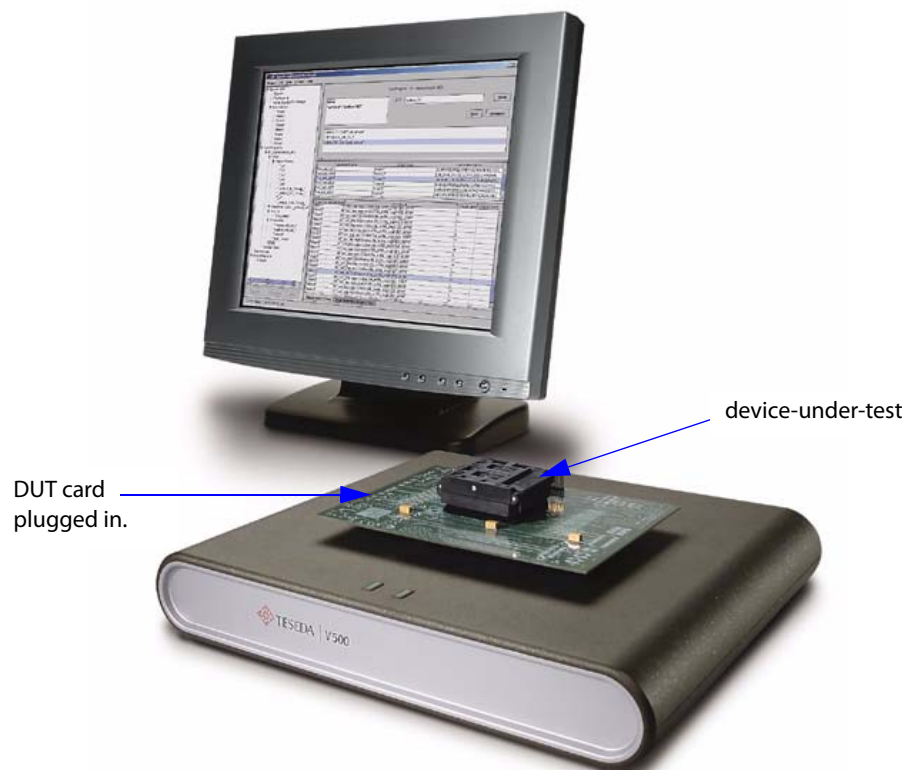


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## Introduction

This design guide describes the process and requirements for creating a printed circuit board to accommodate a device-under-test (DUT) that interfaces with the V520 product shown here.

*Teseda V520  
product with  
DUT card attached*



This guide is intended to provide engineers with essential information for designing a DUT card that will work with the Teseda V520. This guide is not intended to be an all-inclusive list for proper design practices. Teseda recommends you employ the best design practices that would produce a reliable design. The following references and Internet URLs link you to key information you can use in your design.

## Books

- Johnson, H. & Graham, M., *High-Speed Digital Design: A Handbook of Black Magic*, 1993, Prentice-Hall, ISBN 0-13-395724-1.
- Ott, H., *Noise Reduction Techniques in Electronic Systems*, 2nd ed., 1988, John Wiley & Sons, ISBN 0-471-85068-3.

## Links

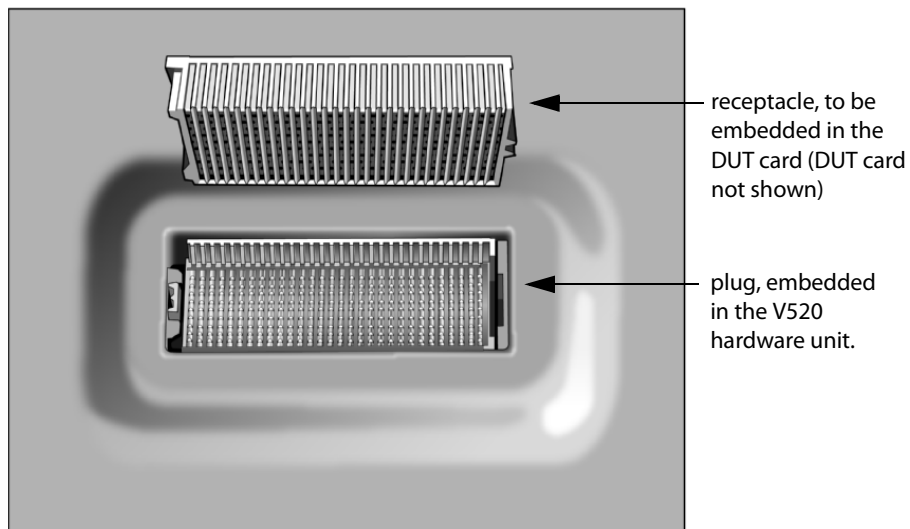
- Portal of links to information about PCB assembly:  
<http://www.smtinfo.net/startpage.html>
- Aries Electronics collet socket connectors (08-0518-11H) series X518; Teseda equivalent part number 430-0017-000: <http://www.arieselec.com>.
- Integrated Circuit Systems component data sheets: <http://www.icst.com/>.  
See the ICS84330 ics84330.pdf data sheet.
- Find information about Teradyne connectors at:  
<http://www.teradyne.com/prods/prodserv.html>
- Teseda V520 information, select: [http://www.teseda.com/prod\\_v520.shtml](http://www.teseda.com/prod_v520.shtml).

## Interface Connectors

The connectors chosen for the DUT card application are Teradyne NeXLeV 300-signal parallel board connectors. Each interface connector contains two parts, a *plug* and a *receptacle*. The DUT card is manufactured with two connector receptacles that mate with two complementary connector plugs in the V520 hardware unit, providing an electrical connection between the tester and the DUT. These are surface-mount components connected to the PCB using ball grid array (BGA) technology. The Teradyne part number for the receptacle connector is **4703105100**. The Teseda part number is **430-0003-000**.

The illustration below shows how one part of a connector (plug) is mounted in the V520 hardware with its complement (receptacle) displayed above. The complement is the part of the connector that is incorporated into the DUT card.

*NeXLeV SMT  
board connectors*



For information on PCB preparation, pad dimensions, via construction, and suggested routing, refer to the *NeXLeV SMT Parallel Board Connector Application Guide*, see the Teradyne website for more information.

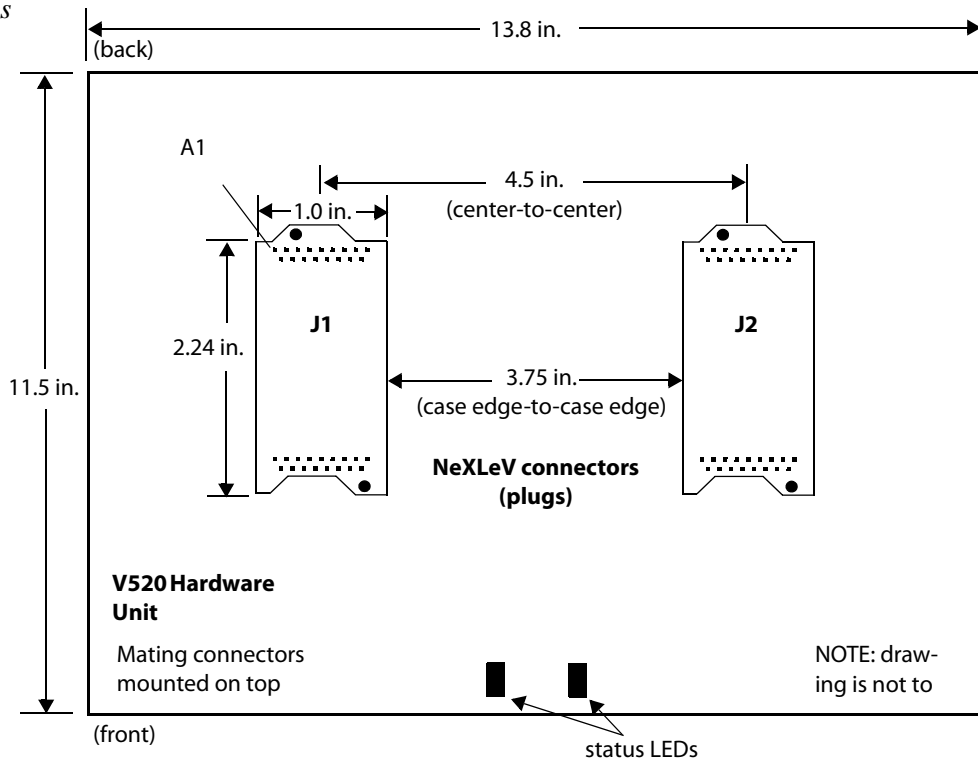
**NOTE:** Make certain to remove the vacuum caps after mounting. Once the connectors are installed on a DUT card, to prevent dust from accumulating in the connectors, be sure to set the DUT card either vertically or with the connector side down, but never facing up. When not in use, DUT cards should be stored in an antistatic bag.

## Form Factor

Board layout details for both the V520 hardware unit and the DUT card, including the spacing and connector dimensions, are shown in the V520 unit and DUT card drawings of this section.

The 4.5 in. center-to-center and 3.75 in. case edge-to-case edge dimensions of the design are critical dimensions. However, the NeXLeV is fairly forgiving of surface-mount placement errors. The connectors can tolerate approximately 0.1mm axial misalignment and 0.2mm vertical misalignment. This drawing shows the J1 and J2 socket locations of the V520 plugs, looking at the top of the V520 hardware unit.

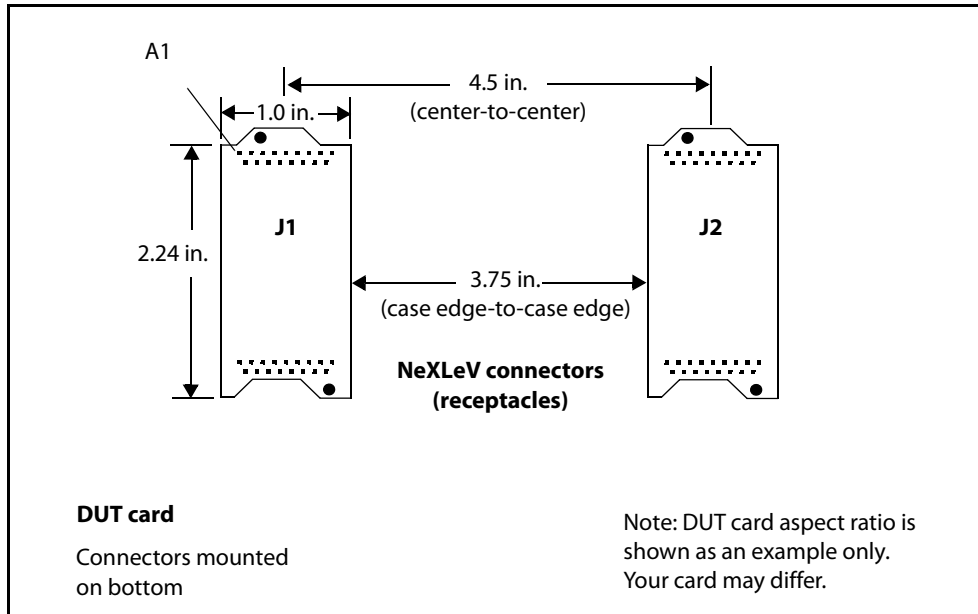
*J1 and J2 socket locations of the plugs on the V520 hardware*



The next drawing shows the J1 and J2 socket locations of the DUT card receptacles. This is the top view of DUT card (looking through the board), connectors mounted on

the secondary side. Note the parallel alignment and part orientation, which prevents mismatch of the DUT receptacles with the V520 plugs.

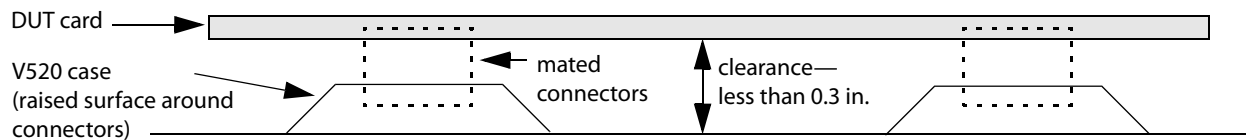
*J1 and J2 socket locations of the receptacles*



The DUT card drawing is a top view; the connectors are actually mounted on the bottom (secondary) side of the DUT card. Connector and spacing dimensions are identical to those as shown for the companion plugs in the V520 unit. The DUT card dimensions themselves are not critical. Nominal dimensions of 9 inches by 6 inches are OK, but your board's form factor may be customized for your design. The main design constraint is that the DUT card should not prevent users from viewing the LED status lights on top of the V520 hardware unit.

The front, side view drawing, below, gives the minimal clearance between the DUT card and the V520 hardware unit. In this drawing, notice the raised surface of the V520 hardware unit and limited clearance between the DUT card and the V520 product. (Components and relative dimensions are not to scale.)

*Front view of the DUT card installed on the V520 hardware unit*



## Domains and Signal Assignments

The V520 uses several different types of pins for applying stimulus to and receiving data from the DUT. There are 300 bi-directional data pins (also referred to as standard pins), 32 clock pins, 16 scan enable pins (or control pins). These include 4 pins for I<sub>DDQ</sub> setup, and 23 pins for signal calibration, reference and debugging. Pin descriptions and terminology relating to the V520 may be found in the V520 Series product section at [http://www.teseda.com/prod\\_v520.shtml](http://www.teseda.com/prod_v520.shtml). These pin resources are described throughout the rest of this section.

The V520 clock, scan enable, calibration, triggering, and data pins are grouped into four domains, A, B, C, and D, organized as described in the table below. Pin voltages are designated for each domain, and all pins within a domain have the same voltage settings. Therefore, pins with different signal levels need to be grouped in different domains. Timing for clocks and scan enables is explained in more detail in sections below.

### Signal assignments

Domain	Clock	Scan Enable	Calibration/Triggers	Data	
A	CLK_AX1	CLK_AX2	SE_A1	CYC_REF_A	DATA_0 through DATA_101
	CLK_AY1	CLK_AY2	SE_A2	CAL_SE_A	
	CLK_AM1	CLK_AM2	SE_A3	CAL_RTN_A	
	CLK_AM3	CLK_AM4	SE_A4	STRB_CAL_A CYC_MRK_A VEC_FAIL_A	
B	CLK_BX1	CLK_BX2	SE_B1	CYC_REF_B *	DATA_102 through DATA_203
	CLK_BY1	CLK_BY2	SE_B2	CAL_SE_B	
	CLK_BM1	CLK_BM2	SE_B3	CAL_RTN_B	
	CLK_BM3	CLK_BM4	SE_B4	STRB_CAL_B CYC_MRK_B VEC_FAIL_B	
C	CLK_CX1	CLK_CX2	SE_C1	CYC_REF_C *	DATA_204 through DATA_299
	CLK_CY1	CLK_CY2	SE_C2	CAL_SE_C	
	CLK_CM1	CLK_CM2	SE_C3	CAL_RTN_C	
	CLK_CM3	CLK_CM4	SE_C4	STRB_CAL_C CYC_MRK_C VEC_FAIL_C	
D	CLK_DX1	CLK_DX2	SE_D1	CYC_REF_D *	None
	CLK_DY1	CLK_DY2	SE_D2	CYC_MRK_D	
	CLK_DM1	CLK_DM2	SE_D3	GLBL_FAIL	
	CLK_DM3	CLK_DM4	SE_D4		

\* DISABLED IN V2.1.2; USE CYC\_REF\_A FOR CALIBRATING ALL DOMAINS.

**NOTE:** Control signal pins for the high-speed clocks, used in BIST applications, are listed in the table [“High Speed Clock Control Signals” on page 15](#). This table maps V520 pin names and numbers to their corresponding ICS84330 pins.

In addition, the power pins and the DC\_PRSENTQ pin (DUT Card Present (Lo) signal) are not assigned to a domain. The DC\_PRSENTQ pin indicates whether the DUT card is connected to the V520 hardware unit. On the DUT card, the DC\_PRSENTQ signal (JT-59) should be connected directly to GND. When the DUT card is plugged into the V520 unit the signal is grounded (Lo). When the DUT card is not present, the signal reads Hi.

See [Appendix A, “Connectors and Pin-Out Signal Mapping”](#) for more details.

## Data pins

The V520 product provides 300 bi-directional data pins spread across three pin domains (A, B, and C) as listed in the table above. Domain D does not contain data pins. Each pin is connected to a 50ohm impedance ( $\pm 20\%$ ) trace and approximately 50pF total capacitance, including pin, connector, vias and trace capacitances. The capacitance applies to the DUT card, without the DUT in place.

The data pins support three different modes of operation: input (drive), output (receive), and high impedance (Z). The mode of any data pin may be changed “on the fly” for a test program run via the appropriate vector data in the test program.

When used in input mode to drive data to the DUT, data pins have a fixed NRZ timing format with data transitions occurring at the beginning of each tester cycle. When used in output mode to receive signals from the DUT, the capture strobe timing edge can be positioned anywhere within the tester cycle. However, all output pins in the same domain must have the *same* strobe timing.

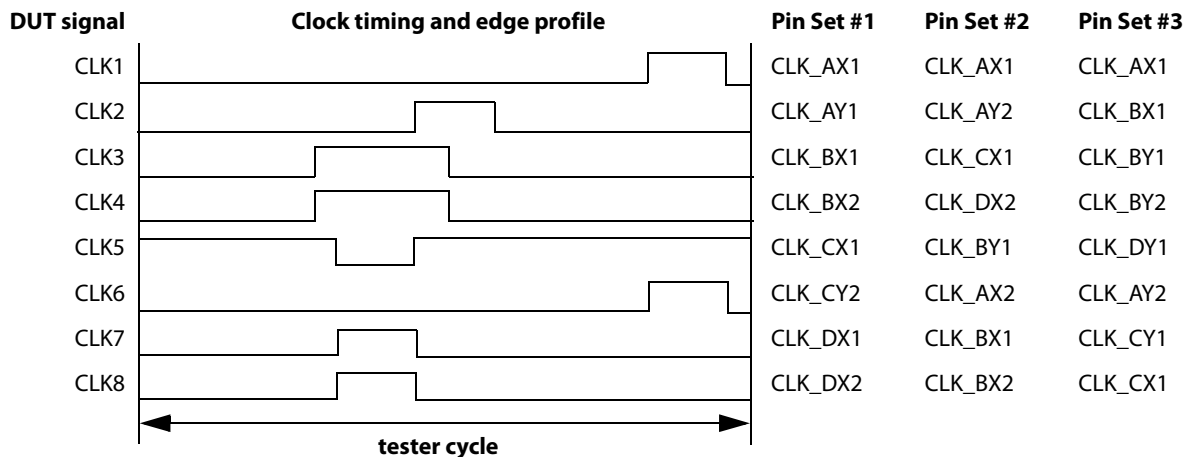
Data pins requiring differing strobe timings must be assigned to different domains. Strobe timing may not be changed during a test program run.

## Clock pins

The V520 uses four pin domains, A, B, C, and D, with two X clock pins and two Y clock pins, plus four M clock pins per domain. However, the clocks are not all independent. Clocks of the same type, either X or Y, within a domain have the same timing/edge settings and polarity, but each clock can be pulsed independently. M clocks are a composite of, and tied to, the edge settings of the X and Y clocks.

### Interdependency of X and Y clocks

Perhaps the best way to explain how X and Y clock domains may be used is with this example of clock assignments using different clock domains.



In this example, the figure shows five different timing edge profiles. The DUT clock signal names CLK1, CLK2, CLK3, ..., CLK8 are arbitrary, made up just for this example. Likewise, the pin sets are arbitrary groupings of clock signal names—such as CLK\_AX1, CLK\_AY1, CLK\_BY1, and so on—organized to illustrate how clock assignments can be made.

As you can see from the figure, CLK7 and CLK8 have the same timing profile, so do CLK3 and CLK4, and CLK1 and CLK6. CLK 5 has the same edges as CLK7 and CLK8 but its timing is inverted. CLK2 also has timing that cannot be matched with any another signal.

Given eight X and Y clocks in four domains, there are many different combinations of tester pin assignments you could make. The example shows three different possible combinations of clock pin sets. Because CLK1 and CLK2 have different timing edges, their respective pin assignments must be made either to different domains or to different X and Y clocks in the same domain.

If CLK1 and CLK2 are assigned to the same domain, then they must be assigned one to an X clock and one to a Y clock (as shown in pin sets 1 and 2). What is not permitted, though, would be to assign CLK1 and CLK2 to, say, CLK\_AX1 and CLK\_AX2 because these X clocks are both in domain A with the same timing profile.

Since CLK3 and CLK4 have the same timing, their signals can be assigned to the X or to the Y clocks in the same domain, or they can each be assigned to different a domain. The same is true of CLK7 and CLK8: these signals can be assigned to the different X or different Y clocks in the same domain, or to either X or Y clocks in separate domains. The criteria for assigning clocks that apply to CLK7 and CLK8 also apply to CLK3 and CLK4.

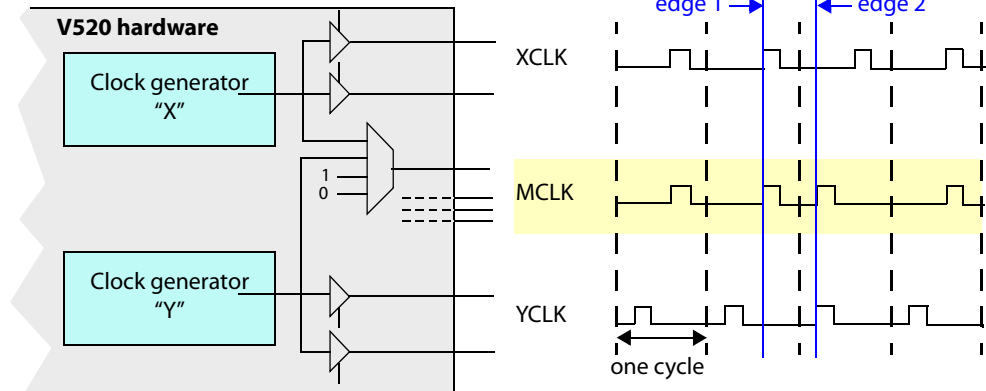
Because CLK5 has distinctive timing, it cannot be assigned to another X or Y clock in the same domain as any other clock. Even though CLK5 has the same timing edges as CLK 7 and CLK8, it is an inverted signal so its timing is different from all other clocks in this example and it must be assigned a different domain, or at least to an unused X or Y clock in the same domain as another clock.

### **M clocks**

The V520 product capabilities include AC scan (scan delay) support. Each AC scan launch/capture clock requires use of the timing/edge sets from a pair of independent X and Y clocks in the same domain. Although, X and Y are independent with respect to each other, M clock timing is a composite of X and Y timing.

The timing edges of M clocks are constrained to be combinations of the edges of either or both X or Y clocks, as illustrated in the following figure. In this figure, the M clock back-to-back "double pulse" is a composite of edge 1 from the XCLK and edge 2 from the Y clock. The MCLK signal can be either XCLK, YCLK, both, or none (OFF).

*M* clock signal multiplexed from X and Y clock timing edges



For more details about how *M* clocks may be used in AC scan analysis, see “Scan Delay Analysis” section in the *V500 Series Teseda WorkBench and Hardware User's Guide*, which may be accessed from the Teseda WorkBench menu by choosing HELP > ONLINE DOCUMENTATION > USER'S GUIDE.

### Clock summary

The arrangement of X, Y and M clock gives you the flexibility to have up to 32 clock pins across the 4 tester domains. Within each domain there are 8 pins and 2 distinct clock waveforms possible via the per-cycle-clock-pin pulse/suppress feature controlled by the vector data in the test program.

Only DUT input pins requiring pulse shaped (SR0 or SR1) stimuli should be mapped to clock pins. Signals with NRZ shape should be mapped to data pins. Also, clock timing cannot be changed during a test program run.

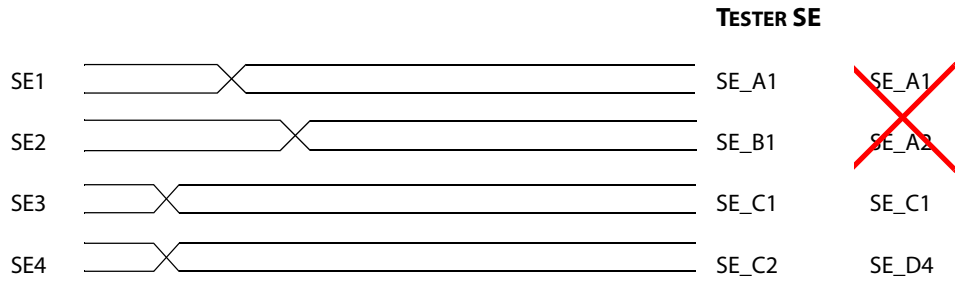
### Scan enable resources

As with clocks, there are four domains, A, B, C, and D, for scan enable signals. Each domain has four DNRZ scan enable (SE) pins per domain, for a total of 16 DNRZ scan enable signals. The edge placements of pins for each domain can be programmed independently, but the edge placement of the scan enable pins within a domain must all be the same. Therefore, up to four scan enable timings may be set.

You can use multiple scan enable pins only for the following reasons:

- ◆ There are other signals on the DUT that must transition at unique times. However, in most cases, all scan enable pins will change state at the beginning of a vector cycle.
- ◆ There is more than one scan enable input to the DUT and it is expected that the scan enables may not all transition simultaneously.
- ◆ A single domain can produce up to four enables with the same timing including combinations of active high or active low signals.

Scan enable pins can be used as NRZ pins as well by setting the transitional delay to 0 ns. The figure below illustrates how scan enable signals can be used in combination.



In this example, there are four DUT scan enable signals, arbitrarily named SE1, SE2, SE3, and SE4. Two of these signals, SE3 and SE4, may be grouped together in the same domain because their timing profiles are identical. You can, therefore, assign one to SE\_C1 and the other to SE\_C2 in the same domain, as shown in the figure, or assign both to alternate signals, such as SE\_C1 and SE\_D4, in different domains. Signals SE1 and SE2, however, cannot share the same domain because their timing profiles are incompatible. Therefore, assigning SE\_A1 and SE\_A2 to these signals won't work. SE1 and SE2 should be assigned to signals in different domains, such as one to SE\_C1 and the other to SE\_D1.

### Summary of requirements for clock and scan enable pins

Clock and scan enable pins operate in an input (drive) mode only. Other requirements for clock and scan enable pins include:

- ♦ V520 clock and scan enable pins cannot be set to high impedance (Z).
- ♦ V520 clock pins cannot be used as NRZ pins, only as SR0/SR1 signals. Defining a pulse from cycle beginning to cycle end would result in unpredictable behavior. The one exception to this rule is when the pin is only set to a single binary value throughout the test program—for instance, always 0. In this case, the pin can behave as a SR0 clock that is always off.
- ♦ Although you can define V520 clock and scan enable pins as InOut in the STIL file, you can only use these pins as input pins in the compiled data that you download and run in the V520 system. This means that you can apply legal force values (suppress or pulse), but you cannot strobe (measure) data—you cannot use an H, L, X, or T on such pins. If an H/L/X/T exists for a vector on any of these pins, you will get Error 1131 during compilation.

A clock pin, for instance, may be designated as an InOut, but in the ATPG tools it is always used as an input pin. This difference in the way the pin is assigned and the way the pin is used, in itself, does not cause a problem with the V520 products.

While DUT clocks in most cases must be connected to V520 clock pins, DUT scan enable signals can often be connected to data pins (if NRZ is okay for scan enable). So, if for some reason a DUT scan enable signal is truly bidirectional, it can be connected to a data pin of the V520 hardware unit.

## Internal Power Supplies

The V520 products use four internal DUT power supplies, two adjustable with a maximum of 2A and two supplies of 100mA each, as listed in the table below. The names used for these supplies correspond to the terminology in the POWER SUPPLY/PIN VOLTAGE view of the Teseda WorkBench (TWB) software. In addition, there are two utility power supplies, one at 5.0V and the other at 3.3V, each limited to 1A. If the current draw for Supply 1 or Supply 2, or for the 5.0V or the 3.3V utility supplies, were to exceed the designated limits, the DUT Power Status LED turns red indicating a fault and a power alarms message displays in the TWB.

Power and ground planes in the DUT card should be connected to appropriate power supplies. The available power supplies, their respective voltage and current ranges, are listed in this table.

TWB power supply name	Voltage range	Current range	V520 connector pins	Action on over-current
Supply 1	1V to 3.8 V	1A to 2A (min to max)	DPS_HC1	Power alarm, run abort, DUT Power Status LED = red
Supply 2	1V to 3.8 V	1A to 2A (min to max)	DPS_HC2	Power alarm, run abort, DUT Power Status LED = red
Supply 3	0.7V to 3.8V	100mA (fixed)	DPS_LC1	Check once at run start. Power alarm, run abort, DUT Power, Status LED = red
Supply 4	0.7V to 3.8V	100mA (fixed)	DPS_LC2	Check once at run start. Power alarm, run abort, DUT Power Status LED = red
<b>DUT card utility supplies</b>				
5.5 V Utility Supply	5.5V (fixed)	1A (max limit) without DCTM 300mA (max limit) with DCTM	5.5_VOLTS	Power alarm, run abort, DUT Power Status LED = red
3.3 V Utility Supply	3.3V (fixed)	1A (max limit) without DCTM 300mA (max limit) with DCTM	3.3_VOLTS	Power alarm, run abort, DUT Power Status LED = red

Although multiple grounds are permitted, all ground signals must connect to a single net. However, you can have a split plane for multiple power signals.

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**CAUTION:** The following key requirements apply:

Do not cascade an internal with an external power supply. Interconnecting these power supplies could overload the DUT card and possibly damage the V520 hardware.

Whenever using an external DUT power supply, limit the supply voltage to 3.8 volts maximum.

Care should be taken to match the logic family voltage of the V520 hardware to the DUT I/O voltage. Voltage and current limits, as well as power delays, are set in the TWB Power Supply/Pin Voltage pane in the Device Under Test Power Supply group.

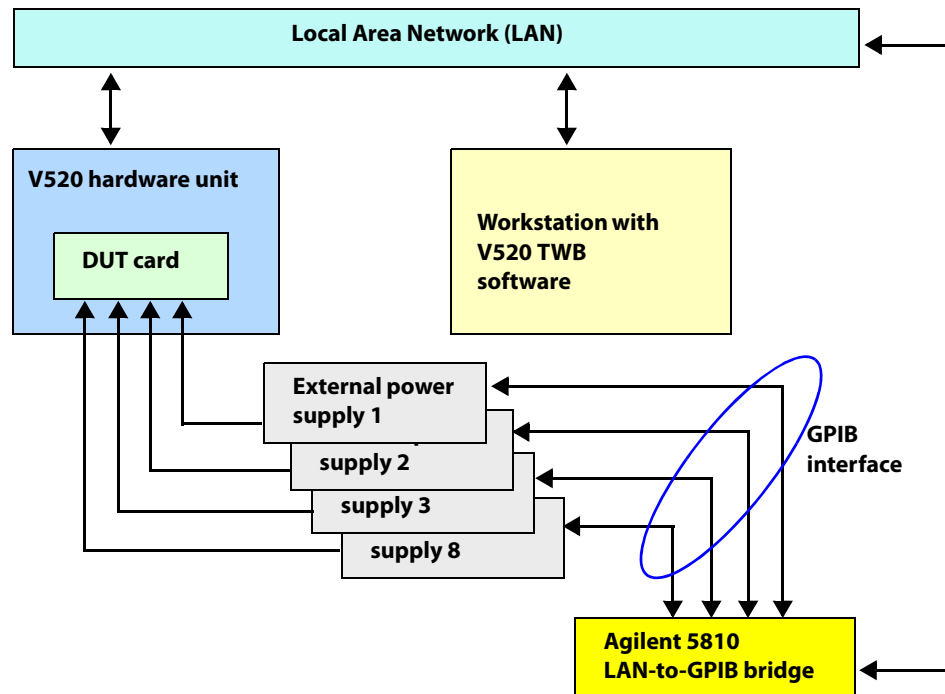
If you anticipate the possibility of an over-voltage risk, contact your Teseda technical representative before you complete your DUT card design.

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## Interfaces for External Power Supplies

A V520 system can control up to eight external GPIB power supplies using the Agilent 5810 LAN-to-GPIB bridge. Any voltage source mode power supply that is GPIB-compatible may be used as long as it provides ability to remotely set the output voltage, limit the output current, and enable/disable the voltage output.

You can place external DUT power connectors on your DUT card and run net traces from your DUT to these external power supply connectors. Teseda suggests that remote sense lines be used, if available, on high current supplies to ensure voltage monitoring at the DUT pins rather than at the supply terminals. The GPIB interface ports of the GPIB power supplies must be be connected to GPIB interface ports on an Agilent 5810 LAN-to-GPIB bridge, configured as shown here.



In the TWB POWER SUPPLY / PIN VOLTAGES details pane you can enter details for how the TWB communicates with these external power supplies. See “Chapter 3, Pin Map, Power Supply and Pin Voltage Configurations” in the *V500 Series Teseda WorkBench and Hardware Guide* for details.

## I<sub>DDQ</sub> Measurement

The V520 product uses the Q-Star QD-1010 module (dimensions of 1.40 in x 1.60 in) to make I<sub>DDQ</sub> current leakage measurements. This module may be mounted, via connectors, on the DUT card in series between the DUT and the V520 hardware unit.

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**NOTE** V520 hardware units may also incorporate QD-1011 modules. Although the QD-1010 and QD-1011 models are functionally equivalent, there may be operational or performance differences that will be addressed in future releases of this manual. See [“Differences between the Q\\*Star QD-1010 and the QD-1011 models” on page 14](#) for a brief comparison.

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Dimensions, pin outs, connector pin locations, notes and other details may be obtained from the QD-1010 data sheet, which can be found at: <http://www.qstar.be>. Also, specifications of the Aries Electronics socket connectors for mounting the QD-1010 to the DUT card may found at <http://www.arieselec.com>. We recommend the Aries 08-0518-11H single-row collect socket, series X518. The Teseda equivalent part number is 430-0017-000.

The QD-1010 is completely controlled from the V520 system, eliminating the need for extra I<sub>DDQ</sub> instrument control signals in the ATPG test program. Specifically no tester data pins are required to drive the QD-1010, making it possible to run ATPG-generated I<sub>DDQ</sub> patterns directly on the V520 system without modification.

### Q-Star QD-1010 connections to the DUT card

There are 16 pins on the QD-1010 module. However, only 9 of these pins are used with the V520 hardware and DUT card. The following table specifies the pin connections to the DUT and the V520 system. See the Q-Star QD-1010 data sheet (<http://www.qstar.be>) for more information on these pins.

<i>QD-1010 pins mapped to the V520</i>	QD-1010 Pin #	Name	Type*	Function	V520 pin #	V520 pin name
	1	MD	I	Mode control	J1-E15	IDDQ1_MD
	3	DUT	O	DUT supply pin	DUT V <sub>CC</sub>	see Appendix A
	5	AGND	S	Monitor ground for DUT, VDUT, and VIDDQ	any GND	see Appendix A
	6	DOUT	O	Pass/Fail flag - Serial Data output	J1-C15	IDDQ1_DOUT
	7	RESET	I	Monitor reset	J1-G15	IDDQ1_RESET
	12	VCC	S	Positive supply voltage	J1-Row 4	5.0_VOLTS
	13	GND	S	Monitor ground	any GND	see Appendix A
	14	VDUT	I	DUT supply reference input	DUT power	see figure below
	16	CLK	I	Clock input	J1-A15	IDDQ1_CLK

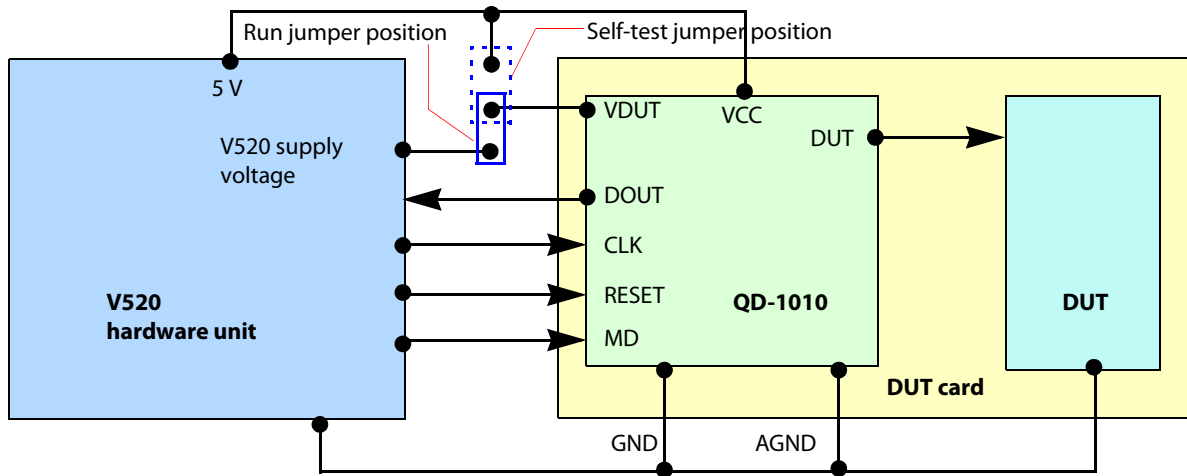
\* O = output, I = input, S = supply

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**CAUTION** Be sure to use proper trace width for QD-1010 5V and DUT power connections to avoid excessive series resistance

---

The following figure diagrams the pin details for connecting the QD-1010 with your DUT card. The QD-1010 has three operating modes: self-test, calibration, and measurement. This drawing also indicates possible connections (jumper configurations) to accommodate these different modes.



### Self-test

The QD-1010 can perform a self-test to verify proper operation. Notification of whether the module passes the self-test is obtained in the TWB. The following criteria apply:

- ♦ The DUT *must not* be installed (it must be taken out of the test circuit).
- ♦ A 5V power supply is needed to supply to the VDUT pin on the QD-1010. This can be an internal V520 supply or an external one. However, the 5V must be disconnected from the DUT *before* the DUT is plugged back into the DUT card.

---

### CAUTION

Although a 5V supply is required for self-test, the DUT *must never* be part of the self-test circuit. Otherwise the DUT is in danger of being damaged.

The diagram above shows a jumper scheme to switch supply voltage between self-test and normal current test operation. To ensure DUT isolation from a 5V circuit, you can incorporate an over-voltage monitoring switch into your DUT card design.

---

### Calibration

To calibrate the QD-1010 for  $I_{DDQ}$  testing, the module must be calibrated individually for each DUT card used. The following conditions apply:

- ♦ The DUT must not be installed (it must be taken out of the test circuit). This arrangement bypasses the DUT circuitry and sets a baseline level for current draw without the DUT in place.
- ♦ The calibration is set up through the TWB. The TWB uses offset values returned from calibration to evaluate  $I_{DDQ}$  results.

## Measurement operation

In measurement mode, the following criteria apply:

- ♦ The QD-1010 must have been calibrated in its host DUT card, at the desired DUT voltage.
- ♦ The DUT needs to be connected on its DUT card.
- ♦ The STIL file imported into the TWB must either contain ATPG-generated  $I_{DDQ}$  measurement points or  $I_{DDQ}$  measurement points must be added or edited via the IDDQ tab in the TWB vector table. See the “Configuring IDDQ Measurements” section in the *V500 Series Teseda WorkBench and Hardware User’s Guide*).

## Differences between the Q\*Star QD-1010 and the QD-1011 models

Compared to the QD-1010, the QD-1011 offers better accuracy and measurement repeatability, reduced interconnect parasitics and lower bypass resistance, reduced multisample measurement times, better data processing capabilities (to support current ratios for example), and more on-board memory. The increased memory is important, for example, when running a pre- and post-stress delta  $I_{DDQ}$  strategy. The the QD-1010 can hold up to 50 measurement results, whereas the QD-1011 can hold up to 500 measurement results The QD-1011 also has additional ground pins.

*QD-1010 and  
QD-1011 multisample  
measurement times*

	Number of Samples	QD-1010	QD-1011
	1 sample	120µs	115µs
	4 samples	190µs	150µs
	16 samples	445µs	290µs

## High-Speed Clocks for BIST Applications

The V520 products support control of up to four high-speed clock channels using the ICS84330 integrated circuit. The high speed clocks (up to 700MHz) are intended for BIST applications where a high-speed clock signal is often required to run the BIST engine. The V520 high-speed clocks are implemented by placing an ICS84330 frequency synthesizer chip on the DUT card and connecting the chip's programming and enable lines to the clock control interface pins of the V520 hardware units.

Clock characteristics	Output Frequency Ranges			
	25MHz to 87.5MHz	87.5MHz to 100MHz	100MHz to 350MHz	350MHz to 700MHz
<b>Min. Setting Resolution, MHz</b> <b>Synchronous</b> (with regard to V520 tester cycle) ■ uses V520 internal clock, at 25MHz reference frequency ■ 300ps max jitter peak-to-peak	0.391MHz	0.781MHz	1.563MHz	3.125MHz
<b>Min. Setting Resolution, MHz</b> <b>Asynchronous</b> ■ uses 10MHz to 25MHz crystal on DUT card for reference frequency ■ 40ps max jitter peak-to-peak	0.25MHz	0.5MHz	1.0MHz	2.0MHz

The previous table lists the high-speed clock modes of operation for the ICS84330 chip. Note that this chip produces a 3.3V LVPECL differential output. An appropriate

buffer chip can be used for translation to a single-ended clock output at logic levels compatible with the DUT clock pin. The minimum setting resolution depends on the frequency range used, as indicated in this table

In the TWB user interface, a menu gives you control of up to four ICS84330 synthesizers (see [“Links” on page 2](#)). Here, you can enable or disable each high-speed clock and set its output and reference frequencies as well as the  $V_{CO}$  reference voltage. High-speed clock pins are not included in the pin mapping. These pins are setup outside the context of a STIL test program since there is no waveform timing or pattern data control possible for the high-speed clocks.

---

**NOTE** If the high-speed clock pins are defined in the STIL program, these pins should be mapped as NOT ASSIGNED in a V520 pin map, since they are connected to the frequency synthesizer on the DUT card rather than a generic V520 data or clock pin.

---

### High Speed Clock Control Signals

The table below lists the clock control interface signals used for frequency programming and ON/OFF controls of the high speed clock chips on the DUT card.

#### *High Speed Clock Control Signals*

v520 Pin Name	V520 Pin #	Function	ICS84330 pins
25M_CLKP	J1-L1	V520 25MHz ref clock (diff)	*
25M_CLKN	J1-N1	V520 25MHz ref clock (diff)	*
VCO_SCLK	J1-A3	Serial Data Clock	S_CLOCK (all)
VCO_DATA	J1-C3	Serial Data Line	S_DATA (all)
VCO_SLOAD1	J1-E3	HS Clock 1 Freq Prog Enable	S_LOAD (#1)
VCO_OE1	J1-G3	HS Clock 1 Output Enable	OE (#1)
VCO_SLOAD2	J1-J3	HS Clock 2 Freq Prog Enable	S_LOAD (#2)
VCO_OE2	J1-L3	HS Clock 2 Output Enable	OE (#2)
VCO_SLOAD3	J1-N3	HS Clock 3 Freq Prog Enable	S_LOAD (#3)
VCO_OE3	J1-R3	HS Clock 3 Output Enable	OE (#3)
VCO-SLOAD4	J1-U3	HS Clock 4 Freq Prog Enable	S_LOAD (#4)
VCO-OE4	J1-W3	HS Clock 4 Output Enable	OE (#4)

\* Both the 25M\_CLKP and the 25M\_CLKN signals are differentially routed in a module, such as an MC100EPT21, and the output is connected to the FREF\_EXT pin of the ICS84330.

## Timing Calibration

The V520 uses a manual timing calibration method, employing an oscilloscope and reference and target signals, to adjust for the relative differences in signal path delay from the V520 hardware to the DUT.

The signal path delays include internal signal routing delays within the FPGA designs, path delay from the FPGA pinouts to the V520 NeXLeV connectors, and path delay from the V520 connectors on the DUT card to the DUT pins.

With this calibration process, the V520 system ensures optimum relative edge timing accuracy between clock pins, scan enable pins, and the NRZ drive edges and capture strobes of the data pins.

### V520 timing calibration data

Several dedicated reference and target signals are used in making calibration measurements and adjustments. The V520 systems has a total of 23 total different timing parameters for controlling the tester resources, listed below. The calibration process allows the calibration data (timing offsets) and associated information to be generated for each of these parameters.

---

Clock A X rise timing	Clock C X rise timing	Scan enable A timing
Clock A X fall timing	Clock C X fall timing	Data strobe A timing
Clock A Y rise timing	Clock C Y rise timing	Scan enable B timing
Clock A Y fall timing	Clock C Y fall timing	Data strobe B timing
Clock B X rise timing	Clock D X rise timing	Scan enable C timing
Clock B X fall timing	Clock D X fall timing	Data strobe C timing
Clock B Y rise timing	Clock D Y rise timing	Scan enable D timing
Clock B Y fall timing	Clock D Y all timing	

---

For each tester resource timing parameter, the calibration data values, data type and date of last change are stored as part of the calibration information through the TWB. These calibration data represent adjustments to the parameters used to configure the V520 pin timing. The calibration data are determined one at a time, by making oscilloscope measurements and entering the difference between expected results and actual measurements into the TWB calibration menu. You employ an oscilloscope to measure the time delay between the target and reference signals, and to verify that this delay is within spec.

M clocks are calibrated by separately calibrating the associated X and Y clock timing edges. The TWB user interface allows you to control the M clock mux from the calibration menu so as to be able to drive an M clock path on the DUT card with either the X or Y clock calibration test signal.

A procedure for setting up calibration in the TWB may be found in “Appendix F: V520 Calibration and Timing Specifications” in the *V500 Series Teseda WorkBench and Hardware User's Guide*.

## Timing calibration reference and target signals

In addition to the standard tester resource pinouts, the V520 provides several special purpose signals per pin domain, which are dedicated for calibration use. As indicated in this table, these signals apply to either test or calibration mode.

Pin Map Signal Name *	Active During	Description
CYC_REF_A	Test Mode and Calibration Mode	Global cycle clock and scan enable (control) drive edge for calibration reference, generated from domain A. Effectively a dummy data pin driving 101010... pattern.
CAL_SE_n	Calibration Mode Only	A per domain reference signal for strobe calibration loop-back use only.
CAL_RTN_n	Calibration Mode Only, strobe selected	Return point for strobe calibration loop-back circuit.
STRB_CAL_n	Calibration Mode Only, strobe selected	Calibration strobe captured value. (This signal changes state when the captured data changes).

\*  $n$  = Pin domain letter (A, B, or C). CYC\_REF\_B, CYC\_REF\_C, and CYC\_REF\_D are no longer supported.

You must access two signals on the DUT card, a reference and a target, to calibrate the timing for a selected tester resource.

---

**NOTE** Access to target and reference signals is best done via calibration test points designed into the DUT card and placed *as close a possible* to the DUT pin. (Probing pads inside device sockets is not recommended due to risk of damage to the socket). More information about calibrating may be found in the *V500 Series Teseda WorkBench and Hardware User's Guide*.

---

Signal CYC\_REF\_A is the global reference signal for calibrating clock and scan enable (control) edges. The target signals may be any one of the several signals, in any of the four domains. Target signals include X or Y clocks, scan enable, data strobe (STRB\_CAL\_n) in loop-back mode, or M clock edges tied to the X or Y clocks. A single instance of a reference signal is used for calibrating all domains to provide cross domain calibration.

When calibrating, you make a time delay measurement between the reference signal and the target signal. The measured delay value is entered into the TWB calibration dialog box. A corresponding timing offset, required to calibrate the selected tester resource to achieve the proper reference-to-target timing, is calculated by the TWB.

### Calibration guidelines

The V520 factory calibration typically provides better than  $\pm 1$ ns edge timing accuracy. The factory calibration is done with the DUT card NexLeV connector pads as the calibration reference plane. Signal delays for a typical 50ohm trace on a PCB are about 200ps per inch.

So, for DUT card designs with traces less than 5 inches in length, no user calibration is required to achieve  $\pm 1$ ns accuracy. The most critical pins for a typical DUT card will be the clock pins (M clocks) intended to be used for AC scan (scan delay analysis). In these cases properly designed test points on these pins can provide for up to  $\pm 100$ ps of timing accuracy with user calibration.

Using these guidelines can help in deciding how many calibration reference test points are needed and where to place them on the DUT card.

## Probe point placement on the DUT card

To minimize inaccuracy, probe points for calibration signals need to be placed as close as possible to the DUT socket. How close depends on the socket, and the physical and electrical characteristics of the pins, such as spacing, impedance, capacitance, and other factors. In most cases, though, all the pins will have the same characteristics. If all the probe test points are placed at about the same distance from the socket pins then they should all look the same electrically at the socket pins.

There are many factors to consider when determining how much variance there might be from trace length to trace length. The closer probe points are to the socket the less likely you will see steps on the waveforms due to reflections, and the easier it will be to match trace lengths. On the other hand, you want to have access to the points from the top of the board, so the probe points will have to be some minimal distance away from the pins. You also need to consider that a signal travels on an FR4 board at about 200 ps/in. And since the V520 products have rise and fall times of about 800ps, we suggest that the test points be placed at less than 0.5in from the socket pin so that the “reflection bump” does not happen in the middle of transitions.

So, the recommended length variance from trace to trace is  $\pm 0.2$ in, which corresponds to about 40 ps difference.

## Test points and loop back traces

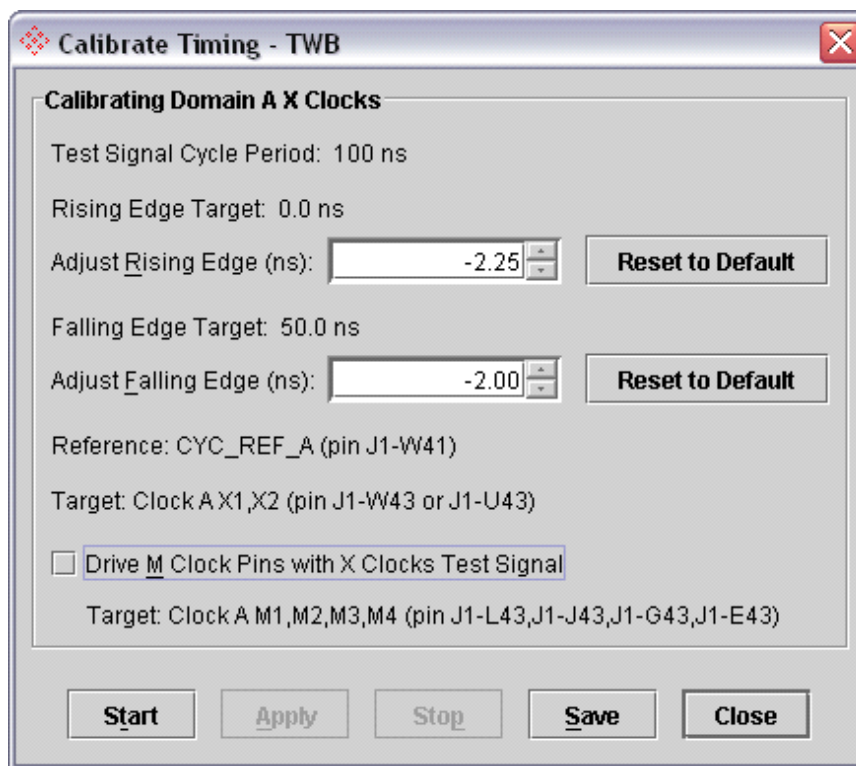
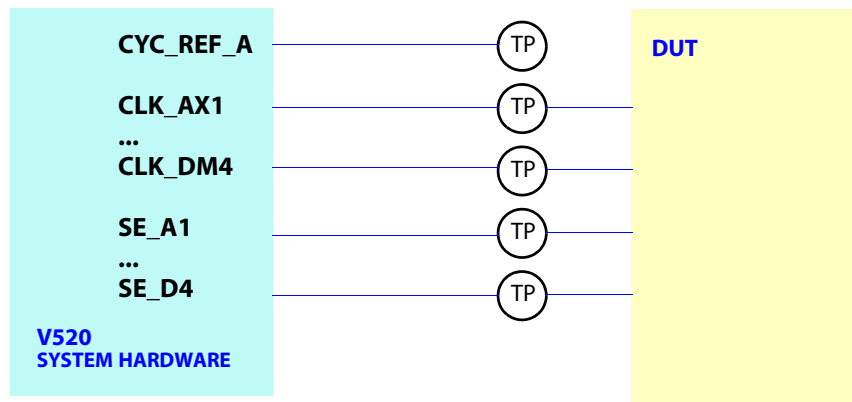
This section explains how to use the test points and loop back traces on a DUT card to enable calibration of clocks, control pins (scan enable), and data strobes on V520 hardware.

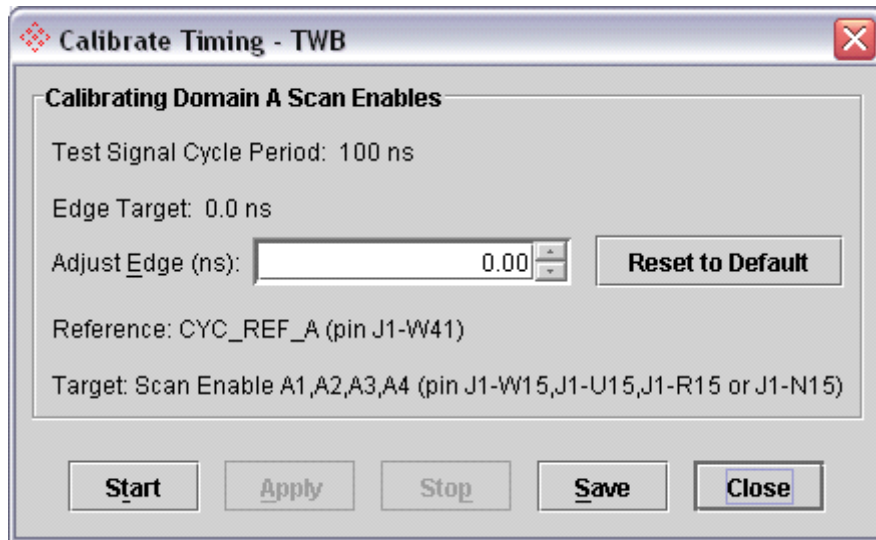
### Clock and scan enable (control) pins

To achieve highest accuracy, all clocks and scan enable signals should have the *same* trace length. All clocks and scan enable signals use the same reference signal (CYC\_REF\_A) for calibration. Therefore, the trace length of CYC\_REF\_A on the DUT card (from connector to test point) should match the length of the clock and scan enable traces from the connector to their respective test points, as illustrated in the diagram on the next page. The test points for clock and scan enable signals should be as close as possible to the DUT pin. The following table summarizes the important considerations for each test element.

*Calibrating clock and scan enable pins*

Test element	Description
Reference	CYC_REF_A This single test point is used for all four domains. The distance from the socket connector (J1-W41) on the DUT card to the test point (TP) should be the same as the distance for the test point on the clock line. <ul style="list-style-type: none"><li>■ For clock pins, the distance is the length from J1-W43 to the clock test point.</li><li>■ For scan enable pins, the distance is the length from J1-W15 to the SE test point.</li></ul>
Target	The actual clock or scan enable pin. <ul style="list-style-type: none"><li>■ For clock pins, there must be one test point per clock used for the particular DUT (up to 32 clock pins). The test point should be located as close as possible to the DUT. Alternately, there may be one test point one per X and Y clock used (for instance just X1 instead of X1 and X2).</li><li>■ For scan enable pins, there must be one test point per scan enable pin (up to 16), as close as possible to the DUT. Alternately, there may be one test point one per domain used (for instance just SE1 instead of SE1, SE2, SE3 and SE4).</li></ul>
Traces	No special traces for calibration.



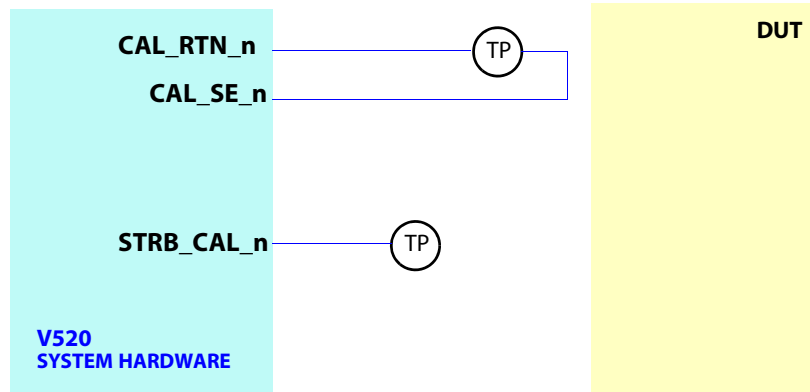
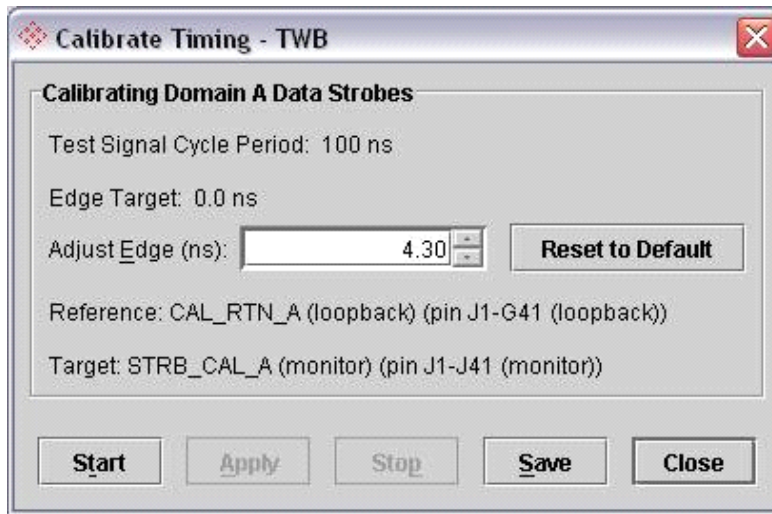


### Data strobe

Data strobing calibration differs from the clock and scan enable calibration according to the description in this table and described in the figure below:

*Data strobe calibration*

Test element	Description
<b>Reference</b>	CAL_RT <sub>n</sub> ...where <i>n</i> represents each domain with data strobes (A, B, and C). The test point can be located anywhere.
<b>Target</b>	STRB_CAL <sub>n</sub> ...where <i>n</i> represents each domain with data strobes (A, B, and C). The test point can be located anywhere
<b>Traces</b>	A loop trace (in the PCB) from CAL_SE <sub>n</sub> to CAL_RT <sub>n</sub> ...where <i>n</i> represents each domain). This means there can be up to three loop traces. A loop should go from the connector on the DUT card and as close as possible to the DUT, and back to the connector, to minimize a route from the connector to the DUT and back. A dedicated test point for CAL_SE <sub>n</sub> is not required.



### Signal / test point summary

Ten signals are involved in calibration (in addition to the up to 32 clocks and 16 scan enable signals). These are `CYC_REF_A`, `CAL_SE_n`, `CAL_RTn_n`, and `STRB_CAL_n` for domains A, B, and C (3 x 3 = 9 signals). Notice that due to the `CAL_RTn_n/CAL_SE_n` loops (and one test point per loop), there is a total of  $1 + 3 + 3 = 7$  test points in addition to the test points required for the clocks and scan enables used (up to  $32 + 16 = 48$ ).

## Triggers and Other Signals

The V520 system has four trigger signals that are controlled through the TWB. These signals, listed in the table below, let you trigger a scope or other external instrument at any specified cycle.

Signal name	Trigger name	Connector pin number
CYC_MRK_A	Trigger 1	J1-A41
CYC_MRK_B	Trigger 2	J2-W41
CYC_MRK_C	Trigger 3	J2-W47
CYC_MRK_D	Trigger 4	J1-A47

For more information about using triggers and pausing tests for making measurements, see the “Set Triggers” section in the *V500 Series Teseda WorkBench and Hardware User’s Guide*.

The table under “[Domains and Signal Assignments](#)” on page 5 mentions `CYC_MRK_n` (where *n* can take on values, A, B, C, or D). These are the four scope triggers that can be activated through the RUN pop-up window in the TWB. Although these signals have nothing to do with calibration, they can be very useful test points, and should be added to most DUT cards to allow triggering of scopes and other external instruments.

Also mentioned in the table are signals `VEC_FAIL_A`, `VEC_FAIL_B`, `VEC_FAIL_C`, and `GLBL_FAIL`. These are monitoring signals that are active when vectors fail for a particular cycle. These have nothing to do with calibration, and are not required for most users.

---

**NOTE** A final signal that needs to be properly routed (but that does not have anything to do with calibration) is the DUT Card Present signal, `DC_PRSNTQ`, which should be connected directly to GND. `DC_PRSNTQ` is low when the DUT card is present, and high when the DUT card is not connected.

---

## Physical Layout Design Considerations

The following information provides general rules. Employing these practices will ensure operational and mechanical reliability of your DUT card. For more detailed information, see “[Books](#)” on page 2 and “[Links](#)” on page 2.

### Layout

- 1 Acquire all component data sheets. These should include both electrical and mechanical information. The documents should also be submitted to the layout designer for library part creation.

---

**NOTE:** The Mentor Graphics/PADS PCB connector footprints can be created from the CAD assembly drawing. Refer to the Teradyne documentation, *NeXLeV SMT Parallel Board Connector Application Guide*.

---

Perform initial component placement using an EDA tool or other drawing editor (such as VISIO or AutoCAD). Locate connectors J1 and J2 on the V520 hardware unit as shown in the figure, “[J1 and J2 socket locations of the plugs on the V520 hardware](#)” on page 3. Lay out the device, or socket, and any additional circuitry to be included on the DUT board. (See [Appendix A, “Connectors and Pin-Out Signal Mapping”](#) for the locations on the connectors of the various signals.)

---

**NOTE:** DUTs and/or their sockets should ideally be centered between the two (J1 and J2) connectors. This arrangement will minimize the electrical lengths of all transmission lines. However, in cases where this is not possible, a location equidistant from both connectors is preferred.

---

- 2 Verify component pin-out and orientation after the PCB library part has been created. This configuration is especially critical for parts such as connectors (mirror image, top/bottom view).

- 3 Determine mechanical constraints such as board dimensions, mounting holes, fixed connector locations, component height restrictions and clearances, keep-outs, layer stack-up and PCB thickness. The underside of the DUT must not contain parts that project vertically beyond the extent of the J1 and J2 receptacles. See the drawing [“Front view of the DUT card installed on the V520 hardware unit” on page 4](#).

---

**CAUTION:** The connectors will fit on the tester in only one orientation. The clip on the end of the receptacle must fit onto the blank end of the plug. Make certain that the connectors are oriented correctly on the DUT card, as shown in [“J1 and J2 socket locations of the receptacles” on page 4](#).

---

- 4 Perform final part placement according to the suggested initial drawing. Ensure compliance with all guidelines and design rules. Placement must adhere to design-for-manufacturability, assembly, and test guidelines where required. See [“Books” on page 2](#) for more information.

---

**NOTE** The spacing between the surface-mount pad arrays is not the same as the spacing between the connectors due to the plastic case surrounding the connector itself.

---

- 5 Define power and ground planes. The planes in the DUT card should be connected to the appropriate power supplies. This system does not provide for split grounds, so only one ground plane is permitted.

- 6 In cases where termination resistors are required to preserve signal integrity, series terminations are recommended. Place the series pass resistor (approximately 33 ohms) on the DUT card as close as possible to the DUT output pin in question. TeseDa recommends avoiding the use of parallel resistance terminations as this may cause excessive loads to be placed on the tester and/or DUT pin drivers, possibly exceeding expected power supply current ranges. For DUT bi-directional pins not predominantly operated as DUT outputs, it is recommended that no DUT side termination resistor be used.

---

**NOTE** The purpose of the series pass resistors is to provide an optimal series termination of approximately 50 ohms. Series termination is used to lessen power consumption and to preserve signal integrity. For clock signals, and certain other signals, however, it may be necessary to use a Thevenin termination. Simulation is recommended to choose optimal resistive value appropriately.

---

---

**NOTE** Check your device specs carefully to determine whether pull-up or pull-down resistors may be required. If they are, you should physically include such resistors in your DUT card design since the V520 products do not provide pull-up or pull-down resistors.

---

- 7 Prepare layout for routing by comparing the schematic netlist against the PCB design netlist. Resolve all net and component package differences.

## Routing

- 1 Identify, then prioritize, which critical signals must be routed first. Signals with similar timing characteristics should be grouped according to function (these would be address, data, control). Re-orient components, if necessary, to optimize for route. Minimize layer switching where possible (to reduce via count). All clocks should be considered part of critical paths in routing.
- 2 Place decoupling capacitors as close as possible to power supply pins with short, wide traces to minimize lead inductance.
- 3 Ensure all signal traces will be impedance-controlled at 50 ohms  $\pm 10\%$ .
- 4 If necessary, route the drive/receive signals to J1 and J2 connector pins on the socket/device following the suggested routing information in the *NeXLeV SMT Parallel Board Connector Application Guide*.
- 5 The netlist, a sample is shown in [“Netlist format”](#), identifies the signals and their connector locations.
- 6 Ensure that all high current traces are wide enough to handle the current.

---

**NOTE** Routing should be optimized to minimize vias, board layers, and signal lengths of critical signals. Such optimization will also reduce fabrication cost of the DUT card.

---

## Netlist format

Netlists used by both Mentor Graphics and PADS can be input in a free-form ASCII format. The netlist format is as follows:

```

Net_Name
Pi n_Name_1 Pi n_Name_2 . . . Pi n_Name_n    (end of line)

```

The example here lists some extracts from a PADS PCB netlist output. See the PADS layout software documentation for details on netlist formatting and output symbols, terminology, and codes.

```

NET LI ST REPORT -- 1105A(XYZLH75401)3. pcb -- Fri Nov 01 14: 37: 02 2002
*SIG 1. 8V-CORE
P25. 1. U          P39. 1. U          P41. 1. U          P28. 1. U
P43. 1. U          P23. 1. U          P37. 1. U          P24. 1. U
DUT1. 75. U       DUT1. 11. U       J6. 2. U           J5. 2. U

*SIG 1. 8V-PLL
J8. 2. U           J7. 2. U           DUT1. 85. U

*SIG 3. 3V-ADC
J12. 2. U          J11. 2. U          DUT1. 97. U
. . .

*SIG D1_SE1
TP1. 1. L          J1. W15. U         DUT1. 30. U

*SIG D1_X2_CLK
TP8. 1. L          DUT1. 86. U        J1. W43. U

*SIG D2_X1_CLK
J2. N43. U         TP7. 1. L          DUT1. 82. U

*SIG D3_X2_CLK
TP2. 1. L          J2. R45. U         DUT1. 62. U

*SIG D4_X1_CLK
TP3. 1. L          DUT1. 67. U        J1. U45. U

*SIG EXTERNAL_PWR_1
J9. 3. U           J10. 3. U          J11. 3. U          J12. 3. U
J3. 1. U           J3. 5. U           J3. 2. U           J3. 6. U
J3. 7. U           J3. 9. U

*SIG EXTERNAL_PWR_2
J5. 3. U           J6. 3. U           J7. 3. U           J8. 3. U
J4. 1. U           J4. 5. U           J4. 2. U           J4. 6. U
J4. 7. U           J4. 9. U

*SIG GND
J1. D02. U         J1. B60. U         J1. F02. U         J1. F14. U
J1. H02. U         J1. H14. U         J1. K02. U         J1. K14. U

```

```

J1. M02. U          J1. K10. U          J1. P02. U          J1. M60. U
. . .
DUT1. 106. U       P44. 1. U          J4. 3. U           J4. 4. U
J4. 8. U           J3. 3. U           J3. 4. U           J3. 8. U
DUT1. 8. U         DUT1. 26. U        DUT1. 14. U        DUT1. 80. U
DUT1. 41. U        DUT1. 48. U        DUT1. 59. U        DUT1. 88. U
DUT1. 84. U        DUT1. 140. U       DUT1. 119. U       DUT1. 127. U

*SIG H_CURR_1
J1. P08. U          J1. T08. U          J1. M08. U          J1. K08. U
J1. H08. U          J1. F08. U          J1. D08. U          J9. 1. U

J10. 1. U           J11. 1. U           J1. B08. U          J12. 1. U
J1. V08. U
. . .
*SIG SCAN144A
DUT1. 87. U         R24. 1. U

```

### Validating the layout

Once you have completed the netlist, carefully check each signal to verify that the connections are correctly mapped and to ensure the circuit design will work in the V520 product. Here is a generalized procedure for validating your circuit design.

- 1 In the Teseda WorkBench, start a new project.
- 2 Import a STIL program for your device.
- 3 Create a pin map file that matches your DUT and the netlist of your DUT card design. A pin map file, corresponding to the board design, may be saved as a .csv file.

You can create a pin map from scratch, or modify a sample pin map using the CREATE SAMPLE PIN MAP functionality in the TWB. See the “Pin Mapping” section in the *V500 Series Teseda WorkBench and Hardware User's Guide* for details on how to create a pin map.

- 4 Import the pin map (.csv file) into the TWB.
- 5 Select the test program and compile; use the VIEW > MESSAGE CONSOLE menu option in the TWB to check for errors or warnings. Modify your pin map and/or DUT card layout as necessary.

The idea is to validate your signal assignments *before* the DUT board design is finalized. This final validation process will verify that you have not made any of the following illegal connections, mapping:

- ♦ An output signal to a tester clock or scan enable pin.
- ♦ A non-clock signal to a tester clock (or vice versa).
- ♦ A non-NRZ input signal to a tester data input.
- ♦ A signal that requires Z state to a tester clock or scan enable pin.
- ♦ Signals with incompatible timing within the same domain.

# Appendix A Connectors and Pin-Out Signal Mapping



---

Here are some general specifications for the connectors.

- The J1 and J2 connectors each consist of staggered row-column arrays. The columns are labeled with alpha characters starting with A, and the rows are numbered 1 through 60. In other words, not all columns are paired with pins, so not all pin numbers are used for each column.
- Columns A, C, E, G, J, L, N, R, U and W are assigned pins from odd-numbered rows, while columns B, D, F, H, K, M, P, T, V and Y are assigned pins from even-numbered rows. This means you can have pin numbers like A1 and A3, but not A2 or A4, and so on. Similarly, pin numbers such as B23 or B37 do not exist.
- There are no columns designated as I, O, Q, S, X, and Z. By convention, these letters are not used.
- All pins in even-numbered rows for columns B, D, F, H, K, M, P, T, V and Y are used for either power or ground, or else reserved for future use. All the pins in each of these even-numbered rows are wired together. There is only a single ground; the design does not allow multiple grounds on a split plane.
- All unassigned pins are designated RESERVED. They are not currently available, but may be implemented in future versions of the V520 and should be left floating for now.

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**NOTE** In the tables of this appendix, the odd rows correspond to the A, C, E,... columns and the even rows correspond to the B, D, F,...columns. The even rows are not listed in the table. The implication is that there is an A1 pin, but no A2 pin, and there is a B2 pin, but no B1 pin, and so on. Since all pins on the *even rows* are shorted together inside the connector, the even-row pins are displayed as a single entry across the spreadsheet columns.

---

## J1 Connector

Tester Rows	J1 tester columns									
	A	C	E	G	J	L	N	R	U	W
1						25M_CLKP	25M_CLKN			
2	GND									
3	VCO_SCLK	VCO_DATA	VCO_SLOAD1	VCO_OE1	VCO_SLOAD2	VCO_OE2	VCO_SLOAD3	VCO_OE3	VCO_SLOAD4	VCO_OE4
4	5.0_VOLTS									
5										
6	GND									
7										
8	SUPPLY 1 (HIGH CURRENT), DPS_HC1									
9										
10	GND									
11										
12	SUPPLY 2 (HIGH CURRENT), DPS_HC2									
13										
14	GND									
15	IDDQ1_CLK	IDDQ1_DOUT	IDDQ1_MD	IDDQ_RESET			SE_A4	SE_A3	SE_A2	SE_A1
16	GND									
17			DATA_0	DATA_1	DATA_2	DATA_3	DATA_4	DATA_5	DATA_6	DATA_7
18	GND									
19							DATA_8	DATA_9	DATA_10	DATA_11
20	GND									
21	DATA_12	DATA_13	DATA_14	DATA_15	DATA_16	DATA_17	DATA_18	DATA_19	DATA_20	DATA_21
22	GND									
23	DATA_22	DATA_23	DATA_24	DATA_25	DATA_26	DATA_27	DATA_28	DATA_29	DATA_30	DATA_31
24	GND									
25	DATA_32	DATA_33	DATA_34	DATA_35	DATA_36	DATA_37	DATA_38	DATA_39	DATA_40	DATA_41
26	GND									
27	DATA_42	DATA_43	DATA_44	DATA_45	DATA_46	DATA_47	DATA_48	DATA_49	DATA_50	DATA_51
28	GND									
29	DATA_52	DATA_53	DATA_54	DATA_55	DATA_56	DATA_57	DATA_58	DATA_59	DATA_60	DATA_61
30	GND									

Tester Rows	J1 tester columns									
	A	C	E	G	J	L	N	R	U	W
31	DATA_62	DATA_63	DATA_64	DATA_65	DATA_66	DATA_67	DATA_68	DATA_69	DATA_70	DATA_71
32	GND									
33	DATA_72	DATA_73	DATA_74	DATA_75	DATA_76	DATA_77	DATA_78	DATA_79	DATA_80	DATA_81
34	GND									
35	DATA_82	DATA_83	DATA_84	DATA_85	DATA_86	DATA_87	DATA_88	DATA_89	DATA_90	DATA_91
36	GND									
37	DATA_92	DATA_93	DATA_94	DATA_95	DATA_96	DATA_97	DATA_98	DATA_99	DATA_100	DATA_101
38	GND									
39										
40	GND									
41	CYC_MRK_A	VEC_FAIL_A	CAL_SE_A	CAL_RTN_A	STRB_CAL_A					CYC_REF_A
42	GND									
43	SE_D4	SE_D3	CLK_AM4	CLK_AM3	CLK_AM2	CLK_AM1	CLK_AY2	CLK_AY1	CLK_AX2	CLK_AX1
44	GND									
45	SE_D2	SE_D1	CLK_DM4	CLK_DM3	CLK_DM2	CLK_DM1	CLK_DY2	CLK_DY1	CLK_DX2	CLK_DX1
46	GND									
47	CYC_MRK_D	GLBL_FAIL								CYC_REF_D
48	GND									
49	DATA_204	DATA_205	DATA_206	DATA_207	DATA_208	DATA_209	DATA_210	DATA_211	DATA_212	DATA_213
50	GND									
51	DATA_214	DATA_215	DATA_216	DATA_217	DATA_218	DATA_219	DATA_220	DATA_221	DATA_222	DATA_223
52	GND									
53	DATA_224	DATA_225	DATA_226	DATA_227	DATA_228	DATA_229	DATA_230	DATA_231	DATA_232	DATA_233
54	GND									
55	DATA_234	DATA_235	DATA_236	DATA_237	DATA_238	DATA_239	DATA_240	DATA_241	DATA_242	DATA_243
56	GND									
57									DATA_244	DATA_245
58	GND									
59					DC_PRSNQ *					
60	GND									

\* The DC\_PRSNQ signal should be connected directly to GND. DC\_PRSNQ is Lo when the DUT card is present, and Hi when the DUT card is not connected.

## J2 Connector

Tester Rows	J2 tester columns									
	A	C	E	G	J	L	N	R	U	W
1										
2	GND									
3	DCRD_ID_0	DCRD_ID_1	DCRD_ID_2	DCRD_ID_3	DCRD_ID_4	DCRD_ID_5	DCRD_ID_6	DCRD_ID_7	DCRD_ID_8	DCRD_ID_9
4	3.3_VOLTS									
5										
6	GND									
7										
8	SUPPLY 3 (LOW CURRENT), DPS_LC1									
9										
10	GND									
11										
12	SUPPLY 4 (LOW CURRENT), DPS_LC2									
13										
14	GND									
15							SE_B4	SE_B3	SE_B2	SE_B1
16	GND									
17			DATA_102	DATA_103	DATA_104	DATA_105	DATA_106	DATA_107	DATA_108	DATA_109
18	GND									
19	DATA_110	DATA_111	DATA_112	DATA_113	DATA_114	DATA_115	DATA_116	DATA_117	DATA_118	DATA_119
20	GND									
21	DATA_120	DATA_121	DATA_122	DATA_123	DATA_124	DATA_125	DATA_126	DATA_127	DATA_128	DATA_129
22	GND									
23	DATA_130	DATA_131	DATA_132	DATA_133	DATA_134	DATA_135	DATA_136	DATA_137	DATA_138	DATA_139
24	GND									
25	DATA_140	DATA_141	DATA_142	DATA_143	DATA_144	DATA_145	DATA_146	DATA_147	DATA_148	DATA_149
26	GND									
27	DATA_150	DATA_151	DATA_152	DATA_153	DATA_154	DATA_155	DATA_156	DATA_157	DATA_158	DATA_159
28	GND									
29	DATA_160	DATA_161	DATA_162	DATA_163	DATA_164	DATA_165	DATA_166	DATA_167	DATA_168	DATA_169
30	GND									

Tester Rows	J2 tester columns									
	A	C	E	G	J	L	N	R	U	W
31	DATA_170	DATA_171	DATA_172	DATA_173	DATA_174	DATA_175	DATA_176	DATA_177	DATA_178	DATA_179
32	GND									
33	DATA_180	DATA_181	DATA_182	DATA_183	DATA_184	DATA_185	DATA_186	DATA_187	DATA_188	DATA_189
34	GND									
35	DATA_190	DATA_191	DATA_192	DATA_193	DATA_194	DATA_195	DATA_196	DATA_197	DATA_198	DATA_199
36	GND									
37							DATA_200	DATA_201	DATA_202	DATA_203
38	GND									
39										
40	GND									
41	CYC_REF_B	STRB_CAL_B	CAL_SE_B	CAL_RTN_B					VEC_FAIL_B	CYC_MRK_B
42	GND									
43	CLK_BM4	CLK_BM3	CLK_BM2	CLK_BM1	CLK_BY2	CLK_BY1	CLK_BX2	CLK_BX1	SE_C3	SE_C4
44	GND									
45	CLK_CM4	CLK_CM3	CLK_CM2	CLK_CM1	CLK_CY2	CLK_CY1	CLK_CX2	CLK_CX1	SE_C1	SE_C2
46	GND									
47	CYC_REF_C	STRB_CAL_C	CAL_SE_C	CAL_RTN_C					VEC_FAIL_C	CYC_MRK_C
48	GND									
49	DATA_246	DATA_247	DATA_248	DATA_249	DATA_250	DATA_251	DATA_252	DATA_253	DATA_254	DATA_255
50	GND									
51	DATA_256	DATA_257	DATA_258	DATA_259	DATA_260	DATA_261	DATA_262	DATA_263	DATA_264	DATA_265
52	GND									
53	DATA_266	DATA_267	DATA_268	DATA_269	DATA_270	DATA_271	DATA_272	DATA_273	DATA_274	DATA_275
54	GND									
55	DATA_276	DATA_277	DATA_278	DATA_279	DATA_280	DATA_281	DATA_282	DATA_283	DATA_284	DATA_285
56	GND									
57	DATA_286	DATA_287	DATA_288	DATA_289	DATA_290	DATA_291	DATA_292	DATA_293	DATA_294	DATA_295
58	GND									
59	DATA_296	DATA_297	DATA_298	DATA_299						
60	GND									

# Appendix B

## Planning a DUT Card Design



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### DUT Card Design and Build Process

This appendix provides a set of checklists you can use to review key elements of your DUT card design, ensuring that all design issues have been considered. For many of the checklist items, there are corresponding cross-references to the V520 documentation that explains the checklist item in more detail, giving you some context for how the DUT card is used with the V520 system.

The following steps are an overview of the design process.

- 1 Identify your DUT and the kinds of DFT evaluations you want to perform using the V520. See the Teseda V520 product page at: [http://www.teseda.com/prod\\_v520.shtml/](http://www.teseda.com/prod_v520.shtml/)
- 2 Review the requirements and guidelines in this document, the *DUT Card Design Guide*, to ensure compatibility between your DUT and the V520.
- 3 Determine how you will integrate the Teradyne NeXLeV connectors into your DUT card to ensure compatibility with the V520.
- 4 Step through the checklists in this appendix to ensure DUT card compatibility with your device. Consider the capacitors, resistors, and connectivity requirements.

Review the DUT card netlist and corresponding pin map. Check your ATPG tool output for appropriate settings (STIL IEEE 1450-1999) to ensure outputs are compatible with the V520 and the Teseda WorkBench. See “Appendix C: Using STIL Files from ATPG Tools” in the *V500 Series Teseda WorkBench and Hardware User’s Guide* for details about how the V520 handles STIL.

- 5 Generate a STIL file for your design to validate your proposed pin mapping. See the [“Validating the layout” on page 26](#) of the *V520 Custom DUT Design Guide* (this document) for more details. Contact Teseda Technical Support if you have questions about compatibility of your DUT design with the DUT card pin mapping.
- 6 Complete the design, placement, and routing of your DUT card. Generate a bill of materials and commission a capable vendor to fabricate your board.

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**NOTE** New information about V520 data pins and corresponding timing, not incorporated into this guide at time of publication, may be found in Chapter 10, “Per Pin Timing” in the *V500 Series Teseda WorkBench and Hardware System Guide*.

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## General information

Gather the following key information and keep it handy for reference as you design and build your DUT card:

---

Teseda technical contact

---

Alternate contact

---

Project/Device name

---

Location of DUT card design files

---

Comments

---

## DFT requirements

Check your intended testing and validation uses for the V520. Your choices here will affect items in the rest of the checklists, below.

- 
- |  |  |
|--|--|
| <input type="checkbox"/> DC scan               | <input type="checkbox"/> BIST                      |
| <input type="checkbox"/> AC scan (scan delay)  | <input type="checkbox"/> JTAG                      |
| <input type="checkbox"/> Failure Analysis (FA) | <input type="checkbox"/> gross functional analysis |
| <input type="checkbox"/> IDDQ                  | <input type="checkbox"/> device characterization   |
- 

## STIL files

Check and verify V520 compatibility with test data for your DUT.

- 
- |  |  |
|--|--|
| <input type="checkbox"/> <b>Source STIL to use</b> — FastScan, TestBench, TetraMAX, TurboScan, others? | Check for version compatibility and possible syntax errors when importing. See “Appendix C: Using STIL Files from ATPG Tools” in the <i>V500 Series Teseda WorkBench and Hardware User’s Guide</i> . |
| <input type="checkbox"/> <b>Unique timesets</b> — single or multiple?                                  | Verify that these system capabilities of your DUT are achievable: clock, enable, and strobe settings.  |
| <input type="checkbox"/> <b>System capabilities</b>  | Verify system capabilities for the following elements. See also “Appendix C: Using STIL Files from ATPG Tools” in the <i>V500 Series Teseda WorkBench and Hardware User’s Guide</i> .                |
| <input type="checkbox"/> Clock count   | Number of clocks and dependencies.   |
| <input type="checkbox"/> Pin count   | Number of data pins.   |
| <input type="checkbox"/> Enable count  |  |
| <input type="checkbox"/> Scan chains   |  |
-

## Power supplies

Identify DUT and DUT board voltage and current requirements.

ITEM	DESCRIPTION
<input type="checkbox"/> <b>Number of supply domains</b>	Determine power requirements. See the “Power Supply Configuration” section of the <i>V500 Series Teseda WorkBench and Hardware User’s Guide</i> .
<input type="checkbox"/> <b>Voltage and current needs of each domain</b>	Determine voltage and current needs of each required supply. See the “Power Supply Configuration” section of the <i>V500 Series Teseda WorkBench and Hardware User’s Guide</i> .
<input type="checkbox"/> <b>Capacitors</b> (bulk and decoupling).	Preferred power decoupling (10 $\mu$ F bulk and 0.01 $\mu$ F decoupling are default values). See <a href="#">“Physical Layout Design Considerations” on page 22</a> of the <i>V520 Custom DUT Design Guide</i> (this document).
<input type="checkbox"/> <b>Power on order and delays</b>	Verify chip needs—always power cores before I/O rings. See the “Power Supply Configuration” section of the <i>V500 Series Teseda WorkBench and Hardware User’s Guide</i> .
<input type="checkbox"/> <b>Common domains from common supply</b>	Check whether multi-sourcing voltage needs in the chip can be derived from a single source. See the “Power Supply Configuration” section of the <i>V500 Series Teseda WorkBench and Hardware User’s Guide</i> , as well as <a href="#">“Domains and Signal Assignments” on page 5</a> and <a href="#">Appendix A, “Connectors and Pin-Out Signal Mapping”</a> of the <i>V520 Custom DUT Design Guide</i> (this document).
<input type="checkbox"/> <b>V520, digital ground only</b>	Some analog tests may be affected because no analog ground is offered. See <a href="#">“Internal Power Supplies” on page 10</a> and <a href="#">Appendix A, “Connectors and Pin-Out Signal Mapping”</a> of the <i>V520 Custom DUT Design Guide</i> (this document).

## Sockets

Complete mechanical drawings of DUT card sockets and ensure these can mate correctly with the V520 connectors

<input type="checkbox"/> <b>Connector/Socket fit</b>	Find information about connector products on the Teradyne site at: <a href="http://www.teradyne.com/prods/prodserv.html">http://www.teradyne.com/prods/prodserv.html</a>
<input type="checkbox"/> Manufacturer	Set fabrication requirements and identify fabricator.
<input type="checkbox"/> Part number	
<input type="checkbox"/> Package type	
<input type="checkbox"/> Socket source	Verify source of this component; to be provided by Teseda or by customer? List bill of materials and source components.
<input type="checkbox"/> <b>Board dimensioning</b>	Review the details in of <a href="#">“Form Factor” on page 3</a> and <a href="#">“Physical Layout Design Considerations” on page 22</a> in the <i>V520 Custom DUT Design Guide</i> (this document).
<input type="checkbox"/> Orientation (of device and socket)	Need to know where pin 1 (or A1) will be located both on the board and seated in the socket.
<input type="checkbox"/> Dimensions	Account for keep out areas such as mounting screws or handles. Some analog tests may be affected because no analog ground is offered. Check for vertical interference between DUT card and V520 surface.
<input type="checkbox"/> Pad pitch (socket and device)	Need this information to verify whether the socket will properly mate with the device.
<input type="checkbox"/> I/F with test board (thru-hole or SMT)	How will the socket mate to the board?

## Pinout

Ensure DUT signals are properly accommodated and connected, and that they map correctly to the V520 Series pins.

ITEM	DESCRIPTION
<input type="checkbox"/> <b>Top or bottom view</b>	Need to know how pins are referenced in the design. (For example, is A2 the second pin over or down?) See <a href="#">“Physical Layout Design Considerations” on page 22</a> of the <i>V520 Custom DUT Design Guide</i> (this document).
<input type="checkbox"/> <b>Pin one</b>	Identify pin 1 for orientation purposes.
<input type="checkbox"/> <b>Unlisted STIL pins</b> (float, ground, other)	If device pins/pads are unaccounted for in the STIL Signals, how should they be accounted for? See “Appendix C, Using STIL Files from ATPG Tools” of the <i>V500 Series Teseda WorkBench and Hardware User’s Guide</i> .
<input type="checkbox"/> <b>Voltage levels for each pin</b>	Currently the V500 Series can accommodate three voltage levels for signals and an additional level for clocks and enables. How shall each pin be classified into domains A,B,C or D for timing and voltage constraints? See the “Pin Voltage Configuration and logic families” section of the <i>V500 Series Teseda WorkBench and Hardware User’s Guide</i> and <a href="#">“Domains and Signal Assignments” on page 5</a> of the <i>V520 Custom DUT Design Guide</i> (this document).
<input type="checkbox"/> <b>Resistors</b> (pull-up, pull-down, or ties between pins)	Identify any special requirements for signals. See <a href="#">“Physical Layout Design Considerations” on page 22</a> of the <i>V520 Custom DUT Design Guide</i> (this document).
<input type="checkbox"/> <b>Power and ground connections</b>	Where are the power connections on the device? See <a href="#">Appendix A, “Connectors and Pin-Out Signal Mapping”</a> of the <i>V520 Custom DUT Design Guide</i> (this document).

## Special requirements

Accommodate any of the following design components in the DUT card design.

<input type="checkbox"/> <b>Trigger points</b>	Four access points used for scope synchronizing and data capture. See <a href="#">“Triggers and Other Signals” on page 21</a> in the <i>V520 Custom DUT Design Guide</i> (this document).
<input type="checkbox"/> <b>Configurable supplies</b> (internal/external)	How will the power needs be met? See <a href="#">“Internal Power Supplies” on page 10</a> and <a href="#">“Interfaces for External Power Supplies” on page 11</a> in the <i>V520 Custom DUT Design Guide</i> (this document).
<input type="checkbox"/> <b>Test points</b>	Custom test points can be included in the DUT card design to access the DUT and corresponding circuitry. See <a href="#">“Physical Layout Design Considerations” on page 22</a> of the <i>V520 Custom DUT Design Guide</i> (this document). <ul style="list-style-type: none"><li><input type="checkbox"/> Clocks</li><li><input type="checkbox"/> Enables</li><li><input type="checkbox"/> Scan chains</li><li><input type="checkbox"/> Other</li></ul> Determine how scan chains, and clock and enable pins, are used with test points.
<input type="checkbox"/> <b>Isolation resistors</b> (ohms)	See <a href="#">“Physical Layout Design Considerations” on page 22</a> of the <i>V520 Custom DUT Design Guide</i> (this document). <ul style="list-style-type: none"><li><input type="checkbox"/> Clocks</li><li><input type="checkbox"/> Enables</li></ul>

- Scan chains
- Other

- 
- Calibration points**      Need to accommodate the four calibration points on the DUT card. See ["Timing Calibration" on page 16](#) of the *V520 Custom DUT Design Guide* (this document).
- 

## V520 options

Decide which of the following modules you'll want to incorporate into your DUT card design.

- 
- AC Scan**      Identify which clock pins will be used for testing. See ["Clock pins" on page 6](#) and ["Timing Calibration" on page 16](#) of the *V520 Custom DUT Design Guide* (this document).
- 
- IDDQ**      Q-Star I<sub>DDQ</sub> module. Identified which supplies to be monitored. See the "Configuration IDDQ Measurements" section in the *V500 Series Teseda WorkBench and Hardware User's Guide*, and ["IDDQ Measurement" on page 12](#) of the *V520 Custom DUT Design Guide* (this document).
- 
- BIST**      High speed clocking and loop tests: up to 300MHz back-to-back pulsing can be achieved using M-Clocks. See the "BIST Analysis and High Speed Clocks" section of the *V500 Series Teseda WorkBench and Hardware User's Guide*, and ["High-Speed Clocks for BIST Applications" on page 14](#) of the *V520 Custom DUT Design Guide* (this document).
-